TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

SAANA KOKKO

ONE SIDED STAR GROUNDED PCB EMC OPTIMIZATION

Master's Thesis

Examiner: University Teacher
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ABSTRACT

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Electromagnetic compliance, EMC, is an important aspect in today's electronic design. Devices should not disturb other devices and also have to work in noisy environment. Tolerable interference emission levels are determined by standards. Electromagnetic interference, EMI, is a process, which involves an interference source, a coupling path and a receiver. Interferences from electronic devices are not only caused by noisy circuits like switching converters and high speed digital circuits, but also non-ideal components. Coupling methods can be divided on four categories: conductive, capacitive, inductive and radiated coupling.

In printed circuit board (PCB) design, electromagnetic interferences can be affected with grounding component placement and routing. Proper PCB design decreases emissions from a device and also inside the device, but on the other hand poor PCB design may cause huge problems. Usually, all design principles can't be implemented and therefore compromises have to be done. Standards define creepage and clearance distances and hence set limitations also directly for PCB design. In PCB, one has to consider also, that manufacturability and design rules may vary for different subcontractors.

Main theories of electromagnetic interference and principles of PCB design are examined through literature review in this thesis. Standards related to examined LED driver and harmonized design rules for all manufacturing plant are also introduced. PCB design's effects on radio frequency interference (RFI) emissions are investigated experimentally using eight test PCBs and one reference PCB. The effect of each design principle is investigated by changing only that feature in each test PCB and by trying to keep the rest of design same reference PCB. Examined features included grounding, tracking and components placement. Measurement process in conformity with CISPR 15 standard is described before measurement results introduction. The effect of the main loop size was not as significant as expected. According to measurement results, the most significant effect on radiated emissions was caused by ground trace width from all examined features.

TIIVISTELMÄ

TAMPEREEN TEKNILLINEN YLIOPISTO
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Nykypäivän piirilevysuunnittelussa sähkömagneettinen yhteensopivuus on tärkeä näkökulma. Laitteet eivät saa häiritä muita laitteita ja niiden tulee myös toimia häiriöllisessä ympäristössä. Standardit määrittelevät sallitut rajat häiriöiden emittoimiselle. Sähkömagneettinen häiriö on tapahtumasarja, jossa tarvitaan häiriölähde, välittäjä ja vastaanottaja. Sähköisten laitteiden aiheuttamat häiriöt eivät aina johdu ainoastaan häiriöllisistä piireistä kuten hakkureista ja korkeataajuisista digitaalipiireistä, vaan myös komponenttien epäideaalisudesta. Kytkeytymismekanismit voidaan jakaa johtuviin, kapasitiivisiin, induktiivisiin ja säteileviin.

Piirilevysuunnittelussa voidaan vaikuttaa sähkömagneettisiin häiriöihin maadoituksella, komponenttien sijoittelulla ja reitityksellä. Hyvä piirilevysuunnittelu vähentää häiriöiden leviämistä niin laitteesta kuin laitteen sisällä. Toisaalta, huono piirilevysuunnittelu voi aiheuttaa suuria ongelmia. Kaikkia piirilevysuunnitteluperiaatteita ei voida toteuttaa ja siksi kompromisseja joudutaan tekemään. Myös standardit vaikuttavat piirilevysuunnitteluun määrittelemällä eriste- ja ryömintävälit. Piirilevysuunnittelussa tulee huomioida myös, että tuotannollisuus ja suunnittelusäännöt vaihtelevat alihankkijoittain.

Tässä diplomityössä on tehty kirjallisuusselvitys sähkömagneettisten häiriöiden pääteorioista ja piirilevysuunnittelun pääperiaatteista. Myös tutkittuun LED-ajuriin liittyvät standardit ja kaikille tuotannoille sopivat suunnittelusäännöt esitellään. Piirilevysuunnittelun vaikutusta radiotaajuisiin häiriöihin tutkitaan kokeellisesti kahdeksalla testipiirilevyllä ja yhdellä referenssilevyllä. Yhden suunnitteluperiaatteen vaikutusta pyritään selvittämään muuttamalla vain yhtä ominaisuutta yhdellä testilevyllä ja pyrkimällä pitämään piirilevy muilta osin samanlaisena kuin referenssipiirilevy. Tutkitut ominaisuudet liittyvät maadoitukseen, reititykseen ja komponenttien sijoitteluun. Standardin CISPR 15 mukainen mittausprosessi esitellään ennen mittaustuloksia. Pääsilmukan koon vaikutus ei ollut niin merkittävä kuin oli odotettu ja mittaustulosten perusteella merkittävin vaikutus säteileviin häiriöihin olikin maadoitusvetojen leveydellä.

PREFACE

This Master's thesis was done at electronic production development department of Helvar Oy Ab in Karkkila during autumn 2013 and spring 2014. The purpose of this thesis was to investigate EMC features of PCBs to improve and expedite PCB design phase. The examiner was Jouko Heikkinen from Department of Electronics and Communications Engineering of Tampere University of Technology and the supervisor was Senior Designer M.Sc. Jari Heine.

I would like to thank Jouko Heikkinen for valuable feedback and being very flexible with schedule. I would like to thank also my supervisor Jari Heine, M.Sc. designer Markku Kuivalainen and PCB Designer Pertti Virta for guidance and patience.

In addition, I would like to thank all my colleagues in electronic production development department for all help and inspiration during this project.

The dearest thanks I would like to present to my family and friends for the support during my studies and this work.

Karkkila, 9th June 2014

Saana Kokko

CONTENTS

LIST OF ABBREVIATIONS

AMN	Artificial mains network
CAD	Computer aided design
CDN	Coupling-decoupling network
CM	Common-mode current or radiation
DC	Direct current
DM	Differential-mode current or radiation
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESD	Electrostatic Discharge
FET	Field-effect transistor
FR4	Flame retardant 4. A common dielectric material for printed circuit boards.
IC	Integrated circuit
LED	Light emitting diode
MELF	Metal electrode leadless face
MOSFET	Metal-oxide-semiconductor field-effect transistor
PCB	Printed Circuit Board
PDF	Portable Document Format
PF	Power factor
PFC	Power factor correction
PSU	Power Supply Unit
PTH	Pin-through hole, Plated-through hole
PTI	Proof tracking index
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root mean square
SELV	Separated Extra-Low Voltage
SMD	Surface mount device
SMT	Surface mount technology

1 INTRODUCTION

Electronic devices are the main reason for electromagnetic interference (EMI). The term EMI is a process, which includes electromagnetic interference's birth, coupling and propagation as well as the unpleasant behavior that it causes. EMI problem may occur, when three elements – source, receptor and coupling path – are present. Electromagnetic compatibility (EMC) is defined as the ability of device to operate in electromagnetic environment without producing unbearable interference for other devices or itself. Device has to also bear interference on defined level. [1] The modern society has become dependent on electronic devices and environment is full of them. Hence, an equipment shall not produce unacceptable interference and be too sensitive to interference. Standards determine acceptable levels for electromagnetic emission. [2]

Design for EMC is often considered as mains filters, shielded boxes and radio engineering. Time and money spent at the earliest possible design phase bring the greatest rewards and lowest cost for EMC or any other criteria. Implementing correct component and printed circuit board (PCB) design procedures can reduce the need for main line filters or shielded enclosure. Time to market and the price of the final device will be decreased with correct design at the component and PCB level. In mass product industry every penny saved from production costs is significant. Poor PCB design may cause interference with the device itself and cause the device to function incorrectly. [3]

This thesis studies theories behind EMI and main PCB design principles for single- and double-sided PCBs through literature. Effects of some PCB design decisions on single-sided LED driver PCB are experimentally examined. The target is to define the most significant details of PCB design to optimize in these particular devices. The second purpose of this thesis is collect together common PCB design principles according to EMC and harmonized design rules for all manufactory plants. Theory is divided on two parts. Chapter 2 introduces reasons for the birth of EMI and coupling methods. Common design principles noticing EMC features are considering in Chapter 3. Chapter 4 represents the examined device and design rules for manufacturability. Measurement procedures and the results are introduced and discussed in Chapter 5. Finally, conclusions of examined PCBs are presented in Chapter 6.

2 THEORY BEHIND EMI AND EMC

Many variables produce EMI, which is why EMI is often considered as difficult to understand and almost impossible to avoid. For a proper design, designer must understand at least on superficial level why and how there is EMI in a circuit and a PCB. In this chapter basic theories behind EMI are introduced.

2.1 Origin of electromagnetic fields

EMI can be explained mathematically with four Maxwell's equations which describe the interaction of electric charges, currents, magnetic and electric fields. Maxwell's first and second equations are derived from Gauss's laws for magnetic and electric fields. Third equation for electric charge is also called as Faraday's law of induction. The fourth law for electric current is based on Ampère's law. Maxwell's equations are too complex for practical use and to be introduced more closely. To briefly summarize, static-accumulation of electric charges produce an electrostatic field, not magnetic field. Electrostatic field stores energy and is the fundamental function of a capacitor. Constant current source creates magnetic field, not electric. This is the basic concept for use of an inductor. Time-varying current produces both electric and magnetic field. [1; 2]

The geometry of a current source has an effect on the radiated signal. Closed loops are magnetic sources and dipole antennas electric sources. A field produced by a loop depends on current amplitude. The field strength is also proportional to the loop area, if the loop trace is much shorter than the wavelength and therefore electrically small. Physical dimensions of the loop determine the resonant frequency of that loop antenna. Commonly, the larger the loop is, the lower frequency is needed for radiation. When the source loop is electrically close, the distance from the loop is less than one-sixth of a wavelength and the magnetic field falls as square of distance. If the distance is more than one-sixth of a wavelength and hence the loop is electrically far, the field is electromagnetic plane wave, which decreases inversely with the increasing distance. The signal from source loop can be observed with a loop antenna, if the polarization of source loop current matches with that of the measuring antenna. [1]

The electric source is modeled by a time-varying electric dipole. When the frequency is high enough to accumulate opposite charges at ends of the trace, the trace forms a dipole antenna. Charges at ends of the trace change with the time-varying current. The electric field depends on four variables. Similarly as the magnetic field, the electric field is proportional to the amplitude of the current flowing in the dipole. If the length of trace is electrically small, the field is proportional to the length of dipole.

The measuring antenna needs to be in the same orientation to the dipole antenna for signal observation. The behavior is similar to the loop source in the far field and field strength decreases inversely with distance. [1]

In electrically small circuits, noise coupling methods can be modeled with equivalent components. Between two conductors, a time-varying magnetic field can be presented by mutual inductance and electric field as a capacitor. [1]

2.2 Hidden characteristics of passive components

Non-ideal behavior of passive components is one reason for EMI. All passive components have hidden characteristics. This means that every passive component has some nature of other passive components and therefore the behavior of the component changes at higher frequencies. [1]

2.2.1 Non-ideal wires and trace

Every wire and trace has hidden parasitic resistance and inductance. This can be modeled with series connected inductor and resistor like in Figure 1 a). Between two trace or leads there is also capacitance. Although this chapter focuses on traces, these principles concern also wires. The main difference between a trace and a wire is shape and it affects shape related features and measures, such as resistance, inductance and capacitance. Calculations for trace impedance and resistance are introduced more closely in Chapter 3.4.

The trace impedance Z contains resistance R and inductive reactance X_L. Inductive reactance can be calculated with equation

$$X_L = \omega L = 2\pi f L \tag{1}$$

where f is frequency and L is inductance. Equations for resistance and inductance are presented in chapter 3.4 Tracking issues. Impedance is defined by

$$Z = R + jX_L = R + j2\pi f L \tag{2}$$

At low frequencies trace is mostly resistive, but at higher frequencies behavior of trace becomes more like inductor and typically above 100 kHz inductive reactance exceeds resistance. A common rule is, that at frequencies higher than the audio frequency range the trace is inductive and also may radiate RF energy and therefore act as an efficient antenna. [1]

The impedance of trace or wire is shown in Figure 1. The continuous line represents the constant impedance of an ideal trace. The impedance of a real trace is drawn with dashed line. The impedance increases with increasing frequency as described above. The impedance has also some resonant frequencies as is drawn in figure. Resonance is

due to capacitance between two traces and often the trace is modeled like a resistor in Figure 1 b).

Capacitor is defined as two parallel plates with a dielectric material between them. Hence, parasitic capacitance occurs always between two conductors, such as a signal trace and ground. [2] The capacitance can be calculated with the parallel plate equation

$$C_L = \varepsilon_0 \varepsilon_r \frac{A}{h} \tag{3}$$

A is the coverage area, h is the distance between traces, ε_0 is the vacuum permittivity and ε_r is the relative permittivity (dielectric constant) of the substrate. Capacitance occurs also between traces on the same layer. Furthermore, capacitive reactance X_C is described by

$$X_C = \frac{1}{2\pi f C} \tag{4}$$

For example, typical double-sided 0.25 mm thick FR4 PCB with 0.035 mm thick, 0.5 mm wide and 20 mm long trace over a ground plane would exhibit a resistance of 9.8 mΩ, an inductance of 20 nH and capacitive of 1.66 pF. [3]

2.2.2 Resistors, capacitors and inductors

Every component has lead-length inductance due to component leads or bond wires in chips. [1] On the other hand, component terminals contain electric charges as similarly as capacitors plates. Every component lead is also resistive. Hence all passive components have parasitic inductance, capacitance and resistance. These hidden features are more significant at high frequencies. These hidden characteristics can be modeled with different combination of passive components as illustrated in Figure 1. The figure also shows low frequency behavior and response in the frequency domain. [2]

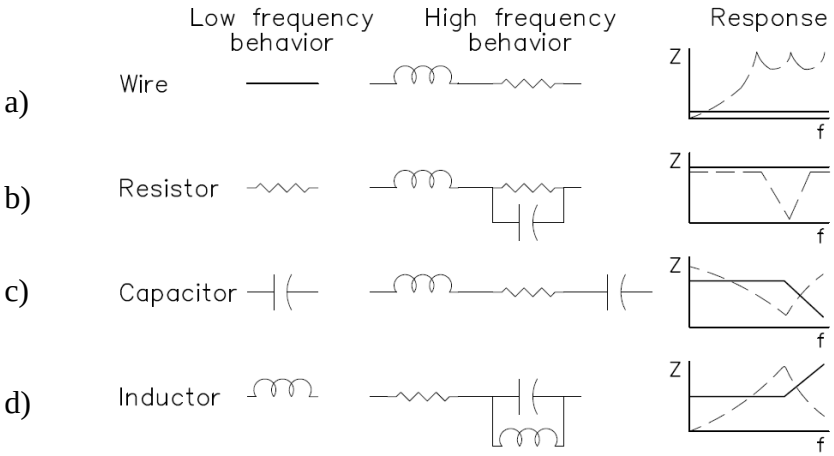


Figure 1. *Hidden characteristics of passive components at high frequencies and response. [1]*

As can be seen in the Figure 1, a resistor acts like in parallel with capacitance across terminals and in series with lead inductance at high frequencies. High frequency features of the resistor depend on material and package. The impedance of resistor drops at the resonant frequency determined by parasitic inductance and capacitance.

Similarly, in the case of an inductor there is capacitance connected in parallel to terminals and lead resistance connected in series. In an inductor there is also capacitance between individual windings. In the ideal inductor, the inductive reactance increases linearly with frequency as described in Equation 1. In reality, the impedance of an inductor increases as the frequency increases until parasitic capacitance becomes dominant and impedance begins to fall.

In the case of a capacitor, the parasitic components (lead resistance and inductance) are connected in series. Reactance of a real capacitor decreases and also the total impedance decreases up to the self-resonant frequency. Above that frequency total impedance begins to increase, since parasitic inductance becomes more significant. [2]

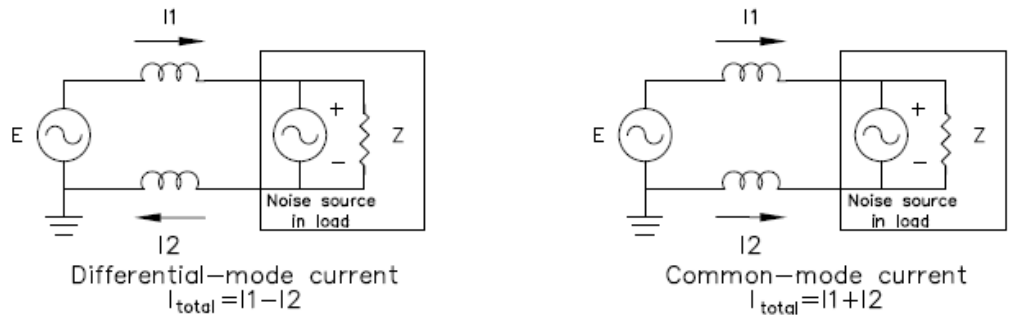
2.3 CM and DM

Common-mode (CM) and differential-mode (DM) currents exist in any circuit and the amount of propagated RF energy is determined by them both. Differential-mode signals carry the information, data or the signal of interest. Common-mode is a side effect of differential-mode. If the two transmission paths aren’t exactly coincident, the radiated emissions of differential-mode currents do not cancel but subtract each other. Conversely, common-mode currents flow at the same direction and emissions are accumulated. Hence, a smaller common-mode current produces the same amount of RF propagated energy than a larger differential-mode current. [1]

Differential-mode current exists on both signal and return paths that are opposite to each other. RF differential-mode current will be cancelled, if the phase shift is precisely 180°. With differential-mode, a source sends current to a load and an equal value of

return current must be present. Standard differential-mode operation is represented by these two equal currents going opposite directions. Differential-mode current configuration is shown in Figure 2 a). On PCB complete electric field capture and magnetic field cancellation cannot be achieved. The remaining fields are the source of differential-mode EMI. Differential-mode EMI and crosstalk can be controlled with proper source control and careful handling of the coupling mechanisms. [1]

The component of RF energy which is present in both signal and return paths, usually in a common phase, is common-mode current. Common-mode signals don't contain useful information. Common-mode current, that causes RF field, is the sum of currents that exist in both signal and return traces. Common-mode current is due to poor differential-mode cancellation, when two transmitted signal paths are imbalanced. Differential currents will not be cancelled out, if they aren't exactly opposite. The uncancelled portion of RF current is common-mode. Even if differential-mode current is fully cancelled, common-mode effects may still be produced by ground bounce and power plane fluctuation. The configuration of common-mode current is shown in Figure 2 b). [1]



a) b)

Figure 2. *Configurations of DM and CM currents. [1]*

Currents' mixing in shared ground or power plane is often the reason for common mode. Common-mode currents will occur when several signals share common areas of the return plane or when return currents lose their pairing with the original path due splits or breaks in planes. Common-mode currents and impedance of planes cause RF transient voltages on the planes. RF transients produce currents in other signal lines or planes that act like antennas to radiate EMI. Common-mode EMI can be prevented with controlling power supply paths and return currents on the board. [1]

2.4 Coupling

Regarding the definition of EMI as introduced in Chapter 1, interference needs a source, a receiver and a coupling path to be a problem. EMC can be improved by removing source, coupling channel or susceptible receptor. Often it is impossible to remove any of the factors entirely, but the effects can be decreased. PCB design affects mostly on

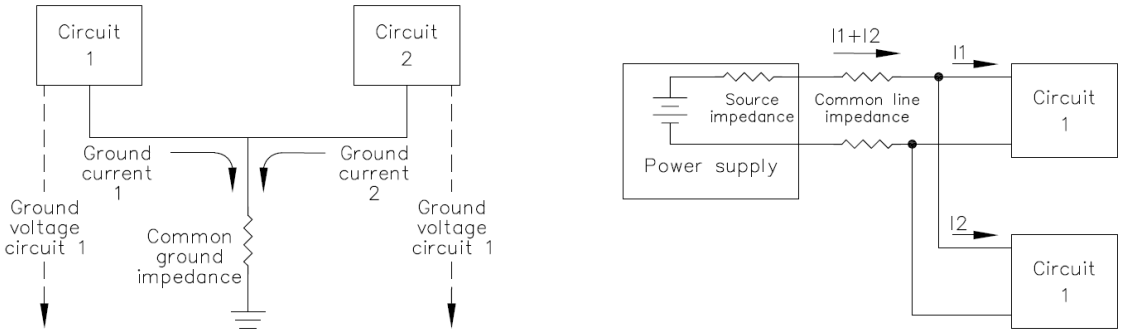
coupling channels and magnitude of interference from sources. Hence, basics of coupling and emission methods need to be understood.

Coupling methods can be divided in four types. Conductive coupling is introduced first in next chapter. In near-field, radiation is considered separately as electric and magnetic fields. Electric and magnetic fields are combined in far-field into and radiation is regarded as electromagnetic radiation. [4]

2.4.1 Conductive coupling

In conductive coupling the noise is transmitted by a conductor, which can be a wire or trace. When the conductor goes through a noisy environment, it can conduct interference to another circuit. If the conductor can't be prevented from picking up noise, the noise should be decoupled before the susceptible circuit.

In coupling through common impedance, currents from different circuits flow through the same impedance. The common impedance is often grounding like in the Figure 3 a). As it is shown in the figure, both circuits are influenced by the voltage drop across the common impedance and that causes them to interfere with each other. Some of the noise signal from the circuit 2 is coupled to the circuit 1 because the ground potential of the circuit 1 is also dependent on ground current 2. [4]



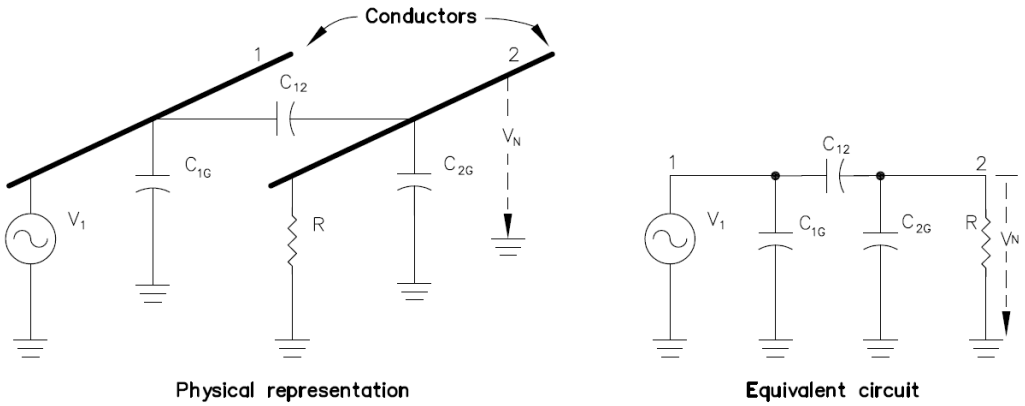
a) b)

Figure 3. *Coupling through common impedance. Common impedance is common ground a) and common supply b).[4]*

The common impedance can be also a supply conductor or other common structure. Another example is shown in Figure 3 b), where two circuits have a common supply. Common impedances are both the internal impedance of the common supply and the supply conductors. If the current of either circuit changes, that will affect the voltage at the other circuit's input. The common impedance decreases if other circuit is closer to the power supply. Then the common impedance from the supply will remain, but the effect of conductors is smaller. [4]

2.4.2 Capacitive coupling

Interaction of electric fields between circuits causes capacitive coupling. Capacitive or electric coupling is the simplest present with two conductors, although the same physical laws are valid with any piece of the circuit structure. The classical presentation of coupling between two wires is shown in the next Figure 4. Before analyze the situation more, some assumptions needs to be made: the cables are electrically short and not shielded by magnetic material, and the skin effect is negligible. [4]



a) b)

Figure 4. *Capacitive coupling between two conductors; a) the physical presentation and b) the equivalent circuit. [4]*

Figure 4 a) shows the physical presentation of capacitive coupling and b) the equivalent circuit. Stray capacitance between conductors is presented as capacitance C_{12} and capacitance between conductor 1 and ground as C_{1G}. C_{2G} is capacitance between conductor 2 and ground including the effect of any circuit connected to conductor and the stray capacitance of conductor 2 to ground. R illustrates the resistance of circuit 2 to ground and isn't a stray component. [4]

Considering the noise voltage produced between inductor 2 and ground, the capacitance directly across source can be neglected. In this case the source is V_1 and capacitance is C_{1G}. The noise voltage can be expressed as follows [4]

$$V_N = \frac{j\omega[C_{12}/(C_{12} + C_{2G})]}{j\omega + 1/R(C_{12} + C_{2G})} V_1 \tag{5}$$

In most practical cases the stray capacitance is higher impedance than R is and assumption can be written as follows

$$R \ll \frac{1}{j\omega(C_{12} + C_{2G})} \tag{6}$$

Therefore, the expression for noise voltage can be reduced to

$$V_N = j\omega R C_{12} V_1 \tag{7}$$

Equation 7 shows clearly how noise voltage depends on the parameters. The noise voltage is directly proportional to resistance R and capacitance C_{12}. These factors can be affected in PCB design. The capacitance C_{12} between conductors can be decreased by increasing the distance between conductors and proper orientation. The effect of spacing is shown in Figure 5.

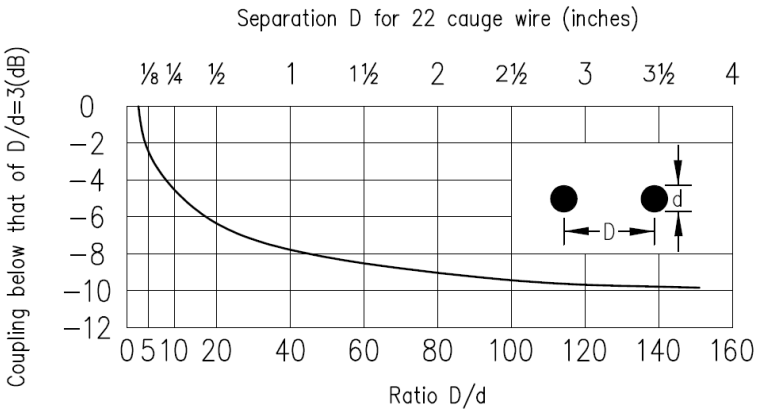


Figure 5. *The relation between conductor spacing and capacitive coupling. [4]*

In Figure 5, 0 dB reference coupling occurs when separation is three times the conductor diameter. As can be seen, the decreasing of coupling slower when the ratio D/d is over 40. The noise voltage is also proportional to magnitude of the voltage V_1 and frequency ($\omega = 2\pi f$), but those values are determined in circuit design. [4]

2.4.3 Inductive coupling

Inductive coupling is caused by interactions of the magnetic fields between circuits. A current of closed circuit produces a magnetic flux ϕ. The flux is proportional to the current I and constant called inductance L. Inductance depends on properties of the medium and geometry of the electrical circuit. For flux can be written [4]

$$\phi = IL \tag{8}$$

The current I_1 in circuit 1, the interfering circuit, produces magnetic flux. If the magnetic flux of circuit 1 penetrates circuit 2, it causes mutual inductance M_{12}. Mutual inductance is defined as follow

$$M_{12} = \frac{\phi_{12}}{I_1} \tag{9}$$

The flux in circuit 2 is described with symbol ϕ_{12} as a result of current in circuit 1. The expression for the noise voltage V_N in a closed loop of area $\bar{A}$ produced by a magnetic field of flux density $\bar{B}$ can be derived from Faraday's law

$$V_N = -\frac{d}{dt}\int_A \bar{B} \cdot d\bar{A} \tag{10}$$

The area $\bar{A}$ and flux density $\bar{B}$ are vectors. If the flux density varies sinusoidally but is constant over the area and the loop is stationary equation 10 comes in form

$$V_N = j\omega BA\cos\theta \tag{11}$$

V_N is the RMS-value of the induced voltage, A is the closed loop area, B is the RMS-value of flux density and θ is the angle on which magnetic field cuts the area. [4]The equation 11 shows, that the noise voltage is proportional to loop area A, flux density B or the angle θ. Flux density can be reduced by increasing the distance between circuits. The term cosθ can be affected with orientation between circuits. Decreasing the area A might be the easiest way to reduce the noise voltage in PCB design. [4]

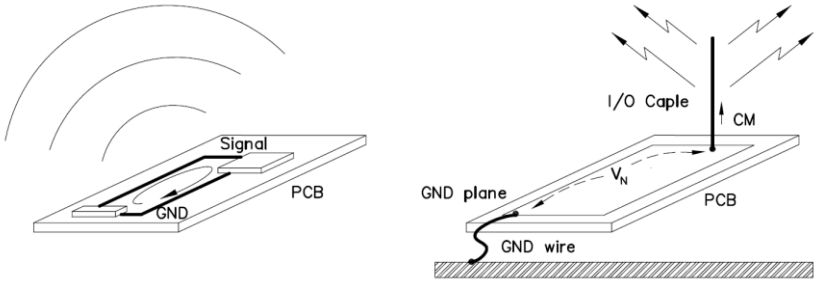
The total magnetic flux ϕ_{12} coupled to the circuit 2, which in this case is the receptor, is here in form $BA\cos\theta$. Hence, the V_N can be represent with the current of the interfering circuit I_1 and the mutual inductance between two circuits [4]

$$V_N = j\omega MI_1 = M\frac{di_1}{dt} \tag{12}$$

The induced voltage is proportional to frequency and mutual inductance M, which describes geometry and the magnetic properties of the medium. [4]

2.5 Radiated emission

Radiated emission can be either differential-mode or common-mode as shown in Figure 6. Current loops, which radiate magnetic fields as small antennas, produce differential-mode radiation, Figure 6 a). Some parts of the systems are at common-mode potential above ground as a result of undesired voltage drops in circuit. External cables connected to the system are driven at this common-mode potential causing common-mode radiation, Figure 6b). [4]



a) b)

Figure 6*. Radiated emission; a) differential-mode radiation from PCB and b) common-mode radiation from system wires. [4]*

The source of differential-mode radiation can be modeled as a small loop antenna. In free space, the electric field strength E at a distance r can be calculated

$$E = 131.6 \cdot 10^{-16}(f^2 AI)\left(\frac{1}{r}\right)\sin\theta \tag{13}$$

where E is in volts per meter and the distance r is in meters. The second term of Equation 13 describes the characteristics of the radiation source, where the frequency f is in hertz, the current I is in amperes and the loop area is in square meters. The last term accounts for the angular orientation of the measuring antenna. The constant accounts the properties of free space as the medium. The maximum radiation is not shape sensitive, hence Equation 13 is valid for any planar small loops. Equation 13 is accurate for electrically small loops, where the perimeter is less than quarter of wave length, and approximate for large loops. [4]

The antenna pattern of small loop antenna is a torus in free space. As shown in Figure 7, the maximum radiation is in the plane of the loop and nulls occur in the direction normal to the loop plane. The electric field is polarized in the loop plane and the maximum field can be detected with an antenna, which is polarized at the same direction. For large loops the radiation pattern shown in Figure 7 doesn't apply. The pattern rotates 90° when a loop perimeter is equal to a wavelength and the maximum radiation occurs in the direction normal to the loop. [4]

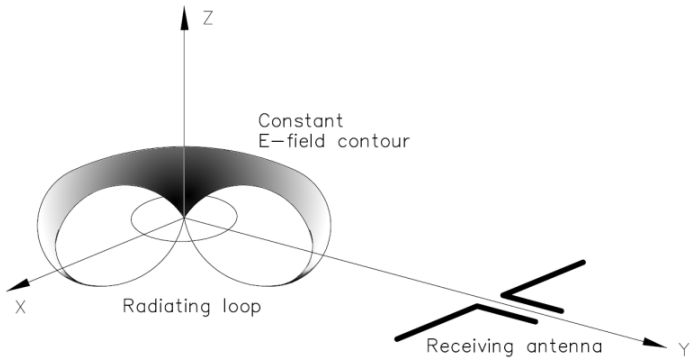


Figure 7. *The antenna pattern of small loop antenna and a receiving antenna. [4]*

Most radiation measurements for electronic devices are made on the ground plane and this can increase measured emission by as much as 6 dB compared to free space. This can be accounted by multiplying Equation 13 with factor of two. With assumption that orientation is for maximum emission, Equation 13 can be rewritten [4]

$$E = 263 \cdot 10^{-16}(f^2 AI)\left(\frac{1}{r}\right) \tag{14}$$

According to Equation 14, the field strength is proportional to the square of the frequency, the loop area and current. Hence, radiation can be controlled by decreasing the magnitude of current, the frequency or the area of the loop.

Common-mode potential, usually the ground voltage, produces common-mode radiation from the cables and the source of emission can be modeled as a short monopole antenna. The magnitude of electric field measured at distance *r* in far field for short monopole antenna of length *l* over a ground plane can be calculated by [4]

$$E = \frac{4\pi \cdot 10^{-7}(fIl)\sin\theta}{r} \tag{15}$$

As in Equation 13, *E* is in volts per meter, *f* is in hertz and *r* is in meters. Common-mode current *I* in the cable, is in amperes and the length of antenna cable, *l*, is in meters. As can be seen from Equation 15, the electric field strength is proportional to the frequency, the common-mode current and the length of antenna. Equation 15 is valid for an ideal antenna and is approximation for a real antenna, which is connected to another piece of device that is grounded or has sufficient capacitance to ground. [4]

Common-mode current is usually the only parameter that can be controlled in design. Current can be controlled by a large common-mode choke in series with the cable and shunting current to ground in schematic design. The common-mode potential can be minimized by proper PCB design. [4]

3 PCB DESIGN FOR EMC

Good PCB design may be the most cost-effective way to achieve EMC compliance, because it is dependent on designer's knowledge, experience and time. If layout design is done correctly there won't be need for additional components. On the other hand, good circuit design can be impaired with poor PCB design. Errors in layout can cause EMC problems, which may not be resolved with additional filters. Remaking PCB design takes time and can delay project, which means extra costs. [3]

Minimizing EMI requires application of many design constrains and so there is no single rule to solve all EMC issues. This chapter introduces some common design rules for layout design, most of which are also good general design principles. The first three are the most important and they should be included in some form in all designs. Since this thesis focuses on products of Helvar, which include only one-sided and double-sided boards, design principles concerning specifically multilayer boards are not therefore discussed in this chapter. Since all of the design principles introduced in this chapter may not be used simultaneously, designers have to make compromises and decisions which are most applicable. [3]

3.1 Segmentation

Segmentation is a design principle, which is also referred as quarantining and functional separation. The principle is to reduce the coupling between circuits by physical separation. The separation depends on the wavelength of signals in each section. The minimum separation should be one-quarter wavelength but usually approximately 5mm gap between circuits is sufficient. [3]

Segmentation is commonly executed by using a moated area around each functional block or circuit. If any ground or power plane is used they should be patterned to prevent noise voltage or a power surge on one block being returned via the ground of another circuit. Grounds and power supplies will meet at one point (usually input) and supply and ground return of each loop can be controlled by separation. The power supply unit (PSU) noise and noise from other circuits can be filtered from circuits by using separated blocks. Separated circuits allow use of smaller and cheaper filtering, which also helps with placement. With separated blocks, filtering of every circuit supply can be optimized according to specified requirements. [3]

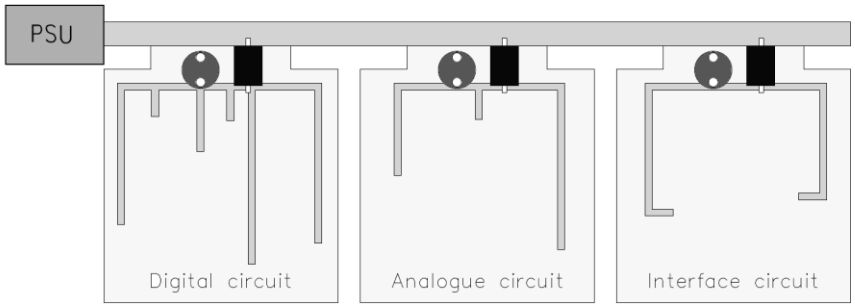


Figure 8. *The principle and the order of separated blocks. [3]*

Blocks can be segmented by function, speed or both. An example of the order of segmented blocks is show in Figure 8. As can be seen, the high speed block is closest to the PSU. The placement of high speed circuit reduces the surge demands being observed on the supplies to slower circuits such as analogue and interface. Naturally interfacing circuits should be near the edge of the PCB when traces have no need to trail across the PCB. Segmentation is preferable even when separation couldn't be implemented. [3]

3.2 Decoupling of local supplies and ICs

Every individual PCB should have its own bypass capacitor at the supply input. The bypass capacitor should be large enough and located as close as possible to the point where power enters the PCB. [3]

Supply noise from one circuit to other is effectively reduced with separated decoupling. A simple LC-filter is often recommendable to reduce crosstalk between circuits. It also prevents circuit noise from getting back to main supply and therefore can remove the need for main filtering. Components for these LC-filters are smaller and cheaper than components that are needed for mains filtering. [3]

Typical value of a bypass capacitor per PCB is between 10 and 100 μF. Bypass capacitors act as a low frequency ripple filters and offer reserve supplies for sudden demands. The best and most effective place for a large bypass capacitor is right at the point where the power enters the PCB. It would be at the socket or wire terminals connecting the PCB with the system PSU. [3]

Decoupling capacitors are smaller than bypass capacitors and they are used to provide a low-impedance route to ground for high-frequency IC switching noise. Typically ceramic decoupling capacitors of few nanofarads also provide a small reserve for transient power demands. The effectiveness of using a decoupling capacitor is easily lost if capacitors are not located near enough to IC's supply pin, as shown in Figure 9. Locating the decoupling capacitor right next to IC reduces the trace impedance to the capacitor, and therefore maintains the effectiveness of the capacitor at high frequencies and with fast edge rates. [3]

The digital system clock is one of the main causes of interference in a digital or a mixed signal system. One way of minimizing the effect is shown in Figure 9. Clock

circuit has a decoupling capacitor next to the supply pin and guard ring. If it is possible, a small bypass capacitor is adequate. [3]

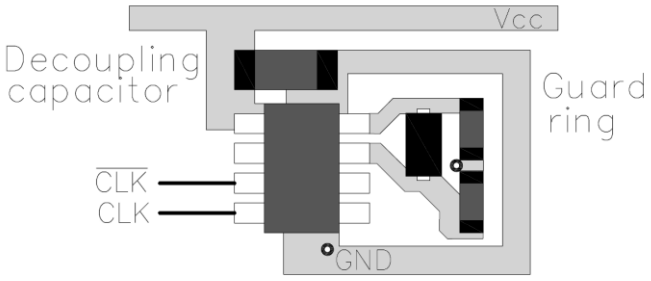


Figure 9. *The location for any decoupling capacitor and the guard ring for a clock clock generating circuit. [3]*

3.3 Grounding

Grounding not only operates as constant potential, but also as failure protection and low impedance return path for current and for interference. The ideal situation would be to have multilayer PCB in which ground and power planes are on separate layers. [4] In this project PCBs are single-sided and since Helvar's products include solely single-sided or double-sided PCBs, multilayer PCBs are not discussed in this thesis.

Grounding techniques aim at minimizing the ground impedance and the size of ground loops from a circuit back to the supply. In the EMC point of view the goaö is not only to minimize resistance, but also inductive reactance of the tracking, which usually dominates the impedance at higher frequencies. Another important point is to control ground current paths. The most suitable grounding technique depends on application, magnitude and frequency of ground currents and construction of equipment. Also designer's knowledge and experience affect the design. [3] Although PCBs in this thesis are star grounded, three different grounding categories are introduced in the following chapters.

3.3.1 Single-point grounding

Principle of single-point grounding is shown in Figure 10. Individual circuit grounds cab be connected in series or in parallel. Single-point suits best for DC and low frequency circuits, below 1 MHz. However, it can be used within the range from 1 to 10 MHz, if the length of the longest ground conductor can be kept under one-twentieth of wavelength to prevent emission and to maintain a low impedance. At high frequencies, the inductances of the ground conductors increase the ground impedance and hence it is undesirable regarding of noise. Controllability of ground current paths is the advantage of single point ground but loop areas may be difficult to be kept small. Therefore this technique is challenging for designer. [2]

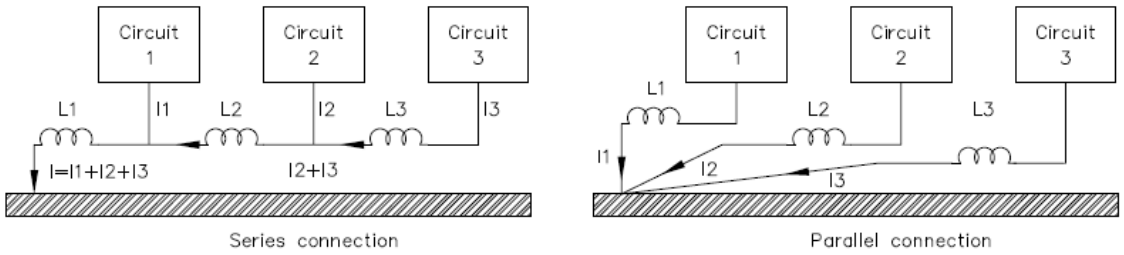


Figure 10. *Single-point grounding. [2]*

Usually single-point ground is formed with signal radials and can be found in dc- and 50/60 Hz power systems, audio circuits and analog instrumentation. [2] In series connected single point grounding, common impedance couples interference strongly. If DC-accuracy is important, the best grounding technique is parallel connected single point, where common impedances are eliminated. [2]

3.3.2 Multi-point grounding

Multi-point ground should be used with digital circuitry and high frequencies. Principle of multi-point grounding is illustrated in Figure 11. In practice, this type of ground is a ground plane or a grid (matrix) and hence it keeps current loops small. Multi-point ground is easy to design and it offers better interference protection than single-point. Multi-point grounds have low ground impedance primarily because inductance of solid copper area is lower than that of narrow PCB trace. Trace inductance depends on trace width and thickness and the additional inductance due to PCB traces is about 4.7 – 7.9 nH/cm. In order to minimize ground impedance, the connection between ground plane and each circuit should be kept short. At very high frequencies the lead inductance allows a voltage potential to be developed across interconnect wire, which is one cause of common-mode current generation. [2]

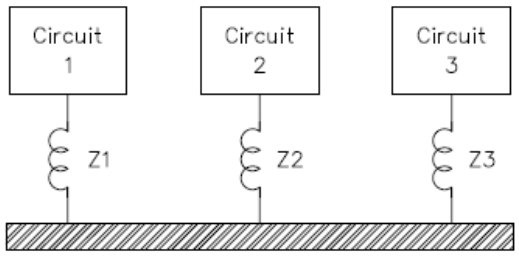
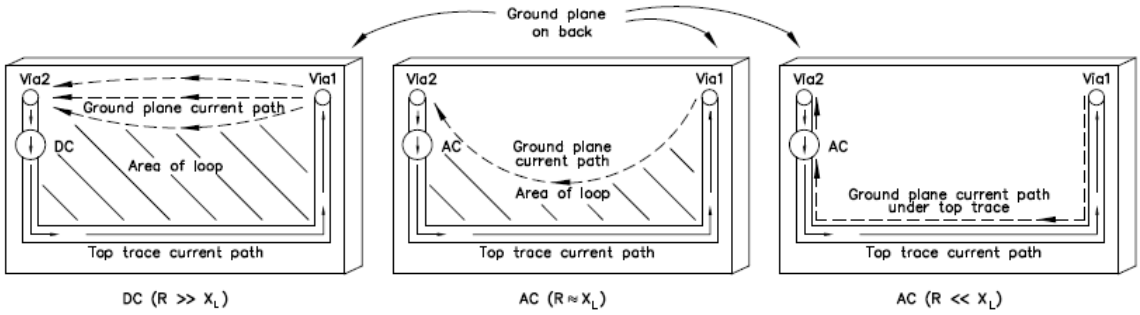


Figure 11. *Multi-point grounding. [2]*

Currents flow along the lowest impedance paths and Figure 12 represents different ground currents flowing in ground plane. As it is shown in Figure 12 a), DC ground current takes the lowest resistance path. The path is quite difficult to presume and the loop area, which effects on inductance, becomes large. Another disadvantage is

common ground impedance when all ground currents follow the same lowest resistance path. Therefore, multi-point ground should be avoided in low frequency circuits. [5]

The resistance of the ground plane causes the currents at low and medium frequencies not to flow under the top trace but neither the shortest way back, as shown in Figure 12 b). High frequency current chooses the lowest inductance path and the ground current flows as close as possible to the signal. The return path is almost under the top trace at frequencies as low as 1 or 2 MHz, Figure 12 c). [5]



a) b) c)

Figure 12. *Different ground current paths; a) DC and very low frequencies, when resistance is dominant. b) Middle frequencies AC, when resistance and inductive reactance are almost equal. c) High frequencies AC, when inductive reactance is dominant. [5]*

Any tracking and big holes should be avoided on ground plane. In Figure 13 trace B is better because it breaks ground plane less than trace A. It is recommendable to use multiple small holes than one large and therefore in the same picture D is better than C. [6]

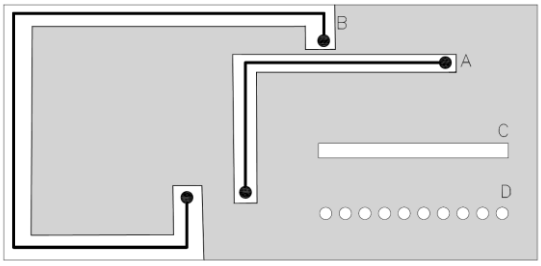


Figure 13. *Tracking and holes on ground plane. Trace B goes do not spilt the ground plane and is better than trace A. Multiple small holes on ground plane are more preferable than one large. [6]*

A ground plane can be replaced with a ground matrix (grid) if there is no chance or will to use a plane. A grid works well with frequencies under 30 MHz. A part f ground matrix is shown in Figure 14. Lines of the grid don’t have to be orthogonal or have the same width. Ground traces should fill empty areas as much as possible and there should be appropriate amount of vias. [4]

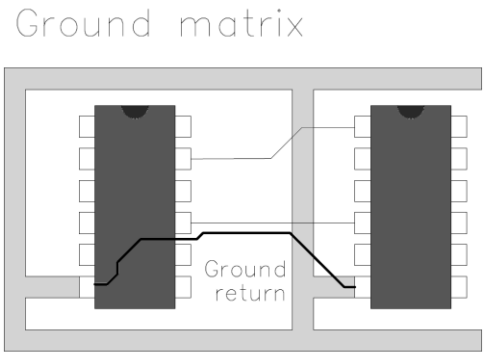


Figure 14. *The ground grid and the ground return for the critical signal. [6]*

Ground patterns make a better contribution, if they are tied at both ends. Returns of critical signals should be done with an own trace next to signal as shown in Figure 14. Open ends shouldn't be left in the grid, because they may increase interference levels. [6]

3.3.3 Hybrid grounding

A hybrid ground is a mix of single- and multi-point grounds. Grounding configuration appears differently at different frequencies: single-point at low frequencies and multi-point at high frequencies. Principle of multi-point grounding is shown in Figure 15. [4]

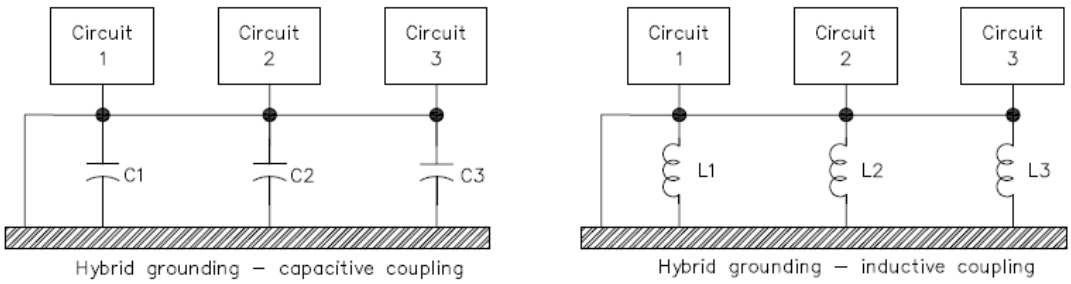


Figure 15. *Hybrid grounding. [2]*

On the same PCB there can be different types of circuits and each of them must be grounded in a manner appropriate for that type of circuit and ground circuits should be tied together, commonly at a single point. [4]

3.3.4 Other grounding considerations

Guarding ring is a ground connected trace which doesn't carry a return current under normal operation. It is tracked usually around PCB or segments within PCB, and often around connectors and input-output circuits. The main purpose of a guarding ring is to be a return source for RF current that produces radiation out of PCB. Guarding ring can be used on one-sided and multilayer PCBs. If a safety ground is available, guarding ring should be connected to it and safety or ESD devices may sink their current via it.

Guarding ring can act as a field fringing sink and it can be used to reduce the segmentation spacing rules. [3]

With single-sided PCB the first consideration should be a wide ground trace plate, in which ground trace will cover as much of the PCB as possible. To prevent unconnected metallized areas, which may reflect signals through board or act like receivers and inject interference capacitively into nearby trace, PCB shouldn't be first covered with ground plane and then etch out the plane for tracking. The star arrangement should be attempted for grounding and for supply, although it can be very difficult with single-sided PCB. [3]

3.4 Tracking Issues

Wires and PCB traces have resistance and at high frequencies also inductance becomes significant. Figure 16 illustrates a method of calculating sufficiently accurate approximation in most cases for the sheet resistance and sheet inductance. [5; 8] Resistivity of copper is 1.678·10-8 Ωm in 20 °C temperature [7] and thickness is usually 0.036 mm. Therefore the sheet resistance of a square is 0.47 mΩ, which can be assumed constant over the PCB. The trace resistance is directly proportional to trace length and inversely proportional to trace width. For example, resistance of 1 mm width and 1 cm long trace is approximately 4.7 mΩ. The minimum trace width for the applications in this thesis is 0.254 mm and resistance for 1 cm long trace is therefore 18.4 mΩ. In conclusion it is quite obvious to keep traces as short and wide as possible. [5; 8]

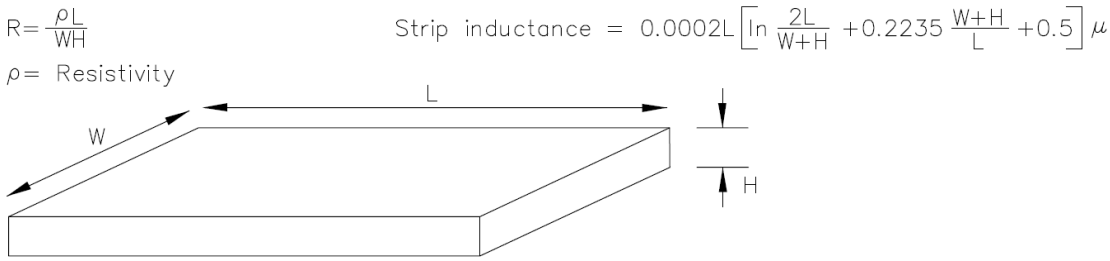


***Figure 16**. Approximation for sheet resistance and inductance. [5; 8]*

Approximation for strip inductance is almost as easy to calculate as resistance as is shown in Figure 16. For 1 mm wide and 1 cm long trace calculated inductance is 6.97 nH. For 0.254 mm wide trace the inductance is 9.49 nH. [5] The frequency at which the inductive reactance of a trace is equal to the resistance is given [7]

$$R = 2\pi f L \tag{16}$$

$$f = \frac{R}{2\pi L} \tag{17}$$

For example, for trace used above, 1 mm wide trace gets frequency a bit under 110 kHz and 0.254 mm wide under 310 kHz. So even for relatively low frequencies the inductance of trace becomes as noticeable as the resistance. [5; 8] The relation between changes of trace width and impedance is illustrated in Figure 17. [3]

As described above the characteristics of trace depends on width and varying trace width may cause reflections and line impedance imbalances. If trace width needs to be changed along a trace, it should be done funneled for smooth impedance change. Funneled trace reduces the possibility of creating a reflection or resonance for interference signals. [3]

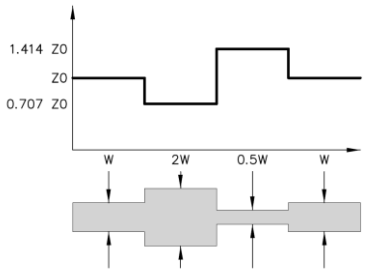
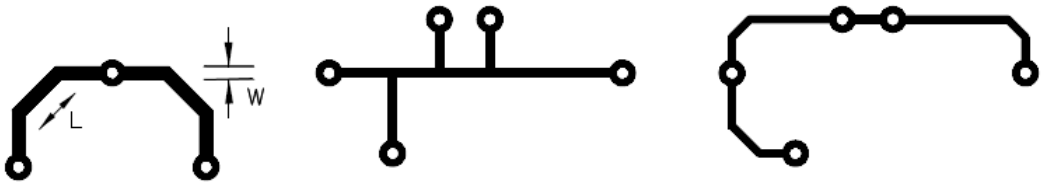


Figure 17. *The impedance change with trace width variation. [3]*

Right angle traces on PCB are rarely used nowadays because sharp corners may cause a field concentration at the inner edge. These field concentrations can cause noise injection into other traces even if they aren't strong enough to fail EMC emission tests. Right angle also creates a small discontinuity in resistance profile of the trace. As shown in Figure 18 a), the mitre should contain at least trace width in length or the radius of a bent should be twice the minimum width. Another and better way to prevent the field concentration is to use round corners but CAD packages do not necessarily support it. [3]



a) b)

Figure 18. *Common tracking considerations; a) the bending mitre should be longer than trace width, L>W b) Continuous trace (right) should be used instead of stubs (left) [3]*

Stubs should be avoided with high frequency and sensitive signal traces. Stubs are potential aerials as well as potential sources of reflections. A star arrangement, in which signal tracking radiates from a single point, should be avoided because it introduces many stubs for signal trace. Although star is often the shortest tracking technique and therefore minimizes delays, it still can produce multiple reflections and radiated

interference and hence may cause more EMI problems than it solves. Therefore smoothly tracking shown in Figure 18 b) is better. [3]

It is fundamental to keep signals and returns close together and to minimize loop areas. It decreases the potential aerial loop size and the capacitive coupling between these traces minimizes bandwidth. [3] Cross-talk involves both capacitive and inductive coupling and can be reduced by increasing the separation between traces, decreasing parallel routed trace lengths and distance between components. [1]

Routing should be started by considering grounding, if ground plane isn't available. In practice, that means at least single-sided and often double-sided boards. Like previously explained, ground and supply traces need to be kept wide and at the same time PCB should be covered with them as far as possible. The next step is to arrange shortest possible traces on PCB for the highest frequency traces and clock or oscillator signals. Clock signal usually goes to every IC in synchronous PCB and tracking could be difficult even it is laid down first. Vias should be avoided because changing a layer may cause delay and it changes the characteristic of inductance. It may be required to use some additional guard rings to minimize loop areas and reduce fringing. The second fastest signals are usually lower order address lines between processors and off-chip memories and then data lines. After high frequency traces, sensitive analogue traces need to lie down and then other signals. The most sensitive and highest frequency traces had to be kept away from power supply lines, because they contain often relatively high amount of noise. Last will come trace for biasing component. For finalizing tracking, unconnected pins and metalized areas should be connected to ground or other convenient point. [3]

Emission within a system inducing interference or producing conducting noise can be a problem, not always the emission out of the system. Even though tracking issues described above seem quite trivial and individually, these design principles may cause only a negligible influence, the thing is that the sum of many of these principles can decrease emission and increase susceptibility of the design. [3]

3.5 Components in PCB design

Most of components are decided at schematic design phase but some component features are good to know also in the PCB design point of view. In this chapter are compared component types and introduced some placement principles.

3.5.1 PTH versus SMD

Electronic components can be divided into leaded or leadless. Leaded components are also known as pin-through hole (PTH) components. In some references PTH stands for plated through holes, nevertheless in speaking of components it means leaded. Surface mount device (SMD), also called surface mount technology (SMT), is better and more descriptive name for a leadless component. PTH technology is older technique where components are placed on opposite side of PCB than tracking. In SMD technology

components are mounted on copper side of PCB. Use of SMD components increase constantly due to growing component density in devices and the drive for smaller devices. [3]

In this thesis there is no reason to cover numerous types of PTH and SMD packages. Only basic passive component package types are introduced aiming to main differences between PTH and SMD components can be compared in EMC point of view. [3]

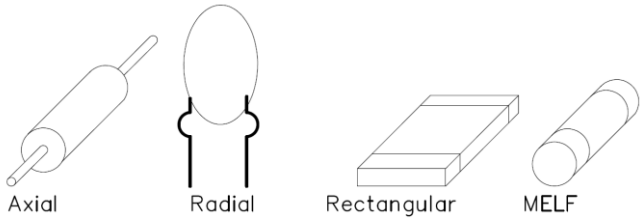


Figure 19. *Most common passive component package types. a) Axial and radial PTH components. b) Rectangular and MELF SMD components. [3]*

Figure 19 illustrates two package types for PTH components a) and SMD components b). Resistors and diodes are typically axial leaded and capacitors are radial leaded. Rectangular package is the most popular in SMD components. Metal electrode leadless face (MELF) components are also used but they aren't as popular as rectangular packages which are handier for automatic placement. [3]

As presented earlier in chapter 2.1.2 components have parasitic features. Parasitic features of PTH components are dominated by lead length, which forms inductor at high frequencies with typical value of 1nH/mm per lead. Therefore, lead lengths should be minimized and component body mounted close to PCB. If component body is far away from the PCB surface also loop area increases. A small, about 4 pF, capacitive effect can also be produced by terminations.[3]

With SMD components designer can't do much, because the shortest possible lead lengths are used already in SMD technology. Also in SMD components the parasitic inductance is dominant in high frequencies, but it is better controlled and more stable than in PTH components. The parasitic inductance is typically 0.5 nH and end termination capacitance is about 0.3 pF. The end termination is usually the dominant parasitic with both thick and thin film SMD resistors at high frequencies. End termination capacitance is about 0.3 pF in small size resistors (0603 and 0805) and about 0.05 pF in 1206. At extremely high frequencies the 0.5 nH termination inductance comes significant. Resistors have also a noise voltage depending on their structure, but it is negligible compared to reactive parasitic. For conclusion, SMD components are generally preferable from EMC viewpoint. [3]

Usually component choices are made in circuit design phase. However, during PCB design there might be situations, where a different package size or type is handier than what it is in a circuit design. Usually with SMD resistors or capacitors, there is no problem to use a bigger package for example to go over a crossing trace. Sometimes a

resistor could be changed from SMD to axial if the alternative is using a jumper or trace would become significantly longer. Jumpers can't be always avoided, but it is more recommendable to use zero ohm SMD resistors, if possible. The jumper or the zero ohm SMD resistor should be inserted preferably in the less sensitive trace.

3.5.2 Component placement

Components should be arranged according to functional blocks or premeditated segmentation. To ease installation, inspection and preparation, it is preferable to place components in rows and columns, whenever it is possible. For the same reason, components should be arranged in the oriented relative to each other. Obliviously, all SMD components should be placed on one side of PCB and PTH components on the opposite side. In wave soldering, it is important to orient all components uniformly and perpendicular to board moving direction. If a component needs to be placed parallel to board moving direction, some additional holes might be needed to achieve proper solder joint. PTH leads can disrupt solder flow to the SMD terminations and hence SMD components shouldn't be surrounded by or placed too near to PTH leads. Component spacing is also important for soldering quality and preventing shadowing. There are some general measurements, but every manufacturer has its own process, which have effect on those. This is discussed more closely in Chapter 4.5, where the main requirements of Helvar's manufacturing and subcontractors are introduced and harmonized. Easy access should be provided for test points, adjustable components, switches et al. Heat sensitive components should be naturally placed away from heat up components and additional copper areas can be added for heat dissipation for hottest components. [3]

4 DRIVER DESIGN AND DEVICES IN EXPERIMENTS

This thesis examines linear LED-driver LL1x23-80-E-CC with single output. This 80W driver is a new product and it has been developed together with mechanically shorter LL1x10-42-E-CC driver. The development was made mainly with the 42W-driver, which was released first for production. Circuits of these drivers are almost the same, but in the 80W driver some of the components are physically bigger because of greater output power. In both drivers the output current can be chosen from three fixed currents or be set with an external resistor. These two drivers made a base for new non-SELV (Separated Extra-Low Voltage) linear LED-driver family. There is already two new products developed in this product family.

4.1 The function of non-SELV LED-drivers

Next graph presents the main function of the drivers introduced above at block diagram level. Blocks are RFI-filter, rectifier, pre-converter and power factor correction (PFC), buck-converter and control. In this chapter the functionality of these LED-drivers is described briefly according to the block diagram.

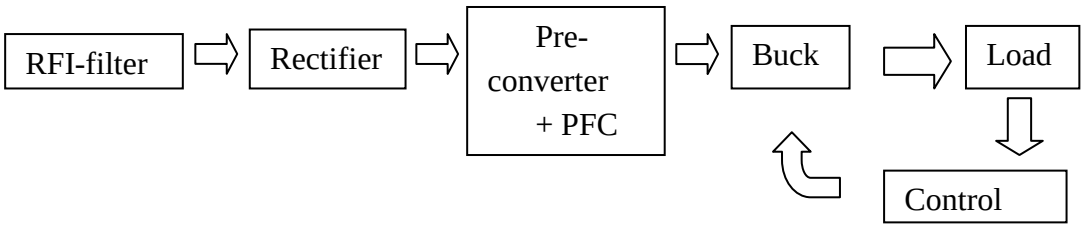


Figure 20. *The block diagram of LL1x23-80-E-CC LED-driver.*

RFI filter protects both network and driver from conductive noise. Filtering conductive noise from the driver to the network improves emission feature and on the other hand filtering improves also immunity of the driver. The filter consists of a common-mode choke, X-capacitors and a Y-capacitor, see Figure 21. The common-mode choke has two wirings with a common ferrite core and it is connected between phase and neutral. The choke acts as an inductance for common-mode signal and for differential-mode signal as a straight wire. X- and Y-capacitors are made especially for network filtering and they tolerate high voltage transients. X-capacitors, C1 and C4, are placed between phase L and neutral N. Y-capacitor C2 is connected to protective ground (ground). Differential-mode noises are filtered with a 3rd degree low-pass filter

created by X-capacitors and stray inductance of the choke. The Y-capacitor and main inductance of the choke acts as a 2nd degree low-pass filter which attenuates common-mode noise efficiently.

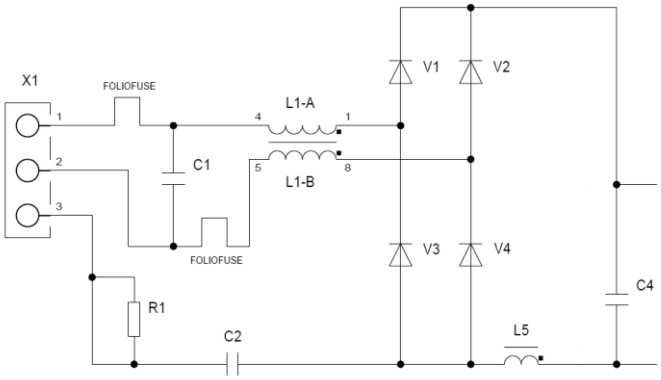


Figure 21. *RFI filter and diode bridge rectifier.*

Figure 21 shows also foil fuses between a network connector and the RFI choke. The foil fuse breaks from peaks of excess current or if driver fails. Network voltage is rectified with a full-bridge diode rectifier, diodes V1, V2, V3 and V4. [9]

The purpose of the pre-converter is to regulate and boost full wave rectified mains voltage suitable for buck circuit. PFC is simplest executed with boost type converter and hence pre-converter is a boost converter. The converter is composed of pre-choke L2, diode V6, capacitor C6 and power MOSFET V5 as a switch. The circuit of the pre-converter is illustrated in Figure 22. When switch (MOSFET) is on, magnetic field of the choke is charged with input current and reverse biased diode isolates output. Output voltage is taken from the big electrolytic capacitor C6. When switch is off, the choke starts to discharge, which causes additional current to flow output. Supply voltage from the diode bridge to boost converter is full wave rectified sine wave, hence a duty ratio of FET can't be constant. In this type of PFC the leading time is theoretically constant, but the discharge time varies. A variable control signal is produced by transition-mode PFC controller IC1 according to actual value of input voltage. The X-capacitor C2 is also significant part of the pre-convert and PFC. C2 converters the RMS-value of supply current from the diode bridge to average-value. Without C2, the PF won't be 1. [9]

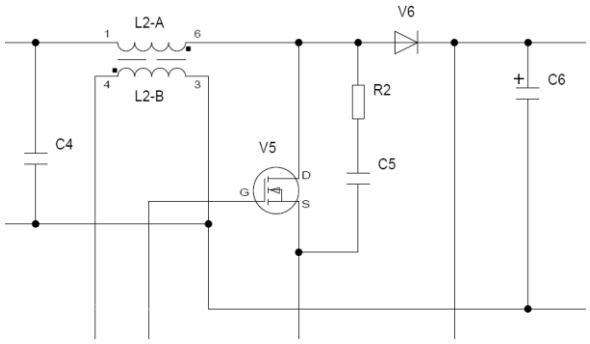


Figure 22. *The pre-converter circuit.*

Non-linear load and high switching frequencies cause current harmonics, which distort shape of current and decreases power factor (PF). [9]Power factor correction is therefore not only required by authorities, but recommended due to power losses. In active PFC the power factor is corrected by switch control. A power factor correction controller obtains information from shapes of input voltage, output voltage and from choke current. The zero point of the pre-choke current is sensed by measuring current of the secondary winding. These input signals are divided with resistors for the voltage to be suitable for the controller. Amplitude of average choke current is set by output voltage and wave form by shape of input voltage. A reference current is two times the average. When choke current reaches the reference the switch is turned off. So step up and step down times of choke current depends on actual value of reference and hence switching frequency becomes variable also. [9]

The circuit of the buck converter is formed by the buck capacitor C13, the buck choke L3 and two MOSFETs V12 and V13. This synchronous rectified arrangement decreases losses and prevents LED from glimmering. LED buck regulator control IC IRS25411 from International Rectifier is used to control MOSFETs. The buck circuit with control IC is represented in Figure 23. Customer chooses the output current by connecting load on predetermined current output or adds an external resistor to a connector next to an output connector to set the output current desirable.

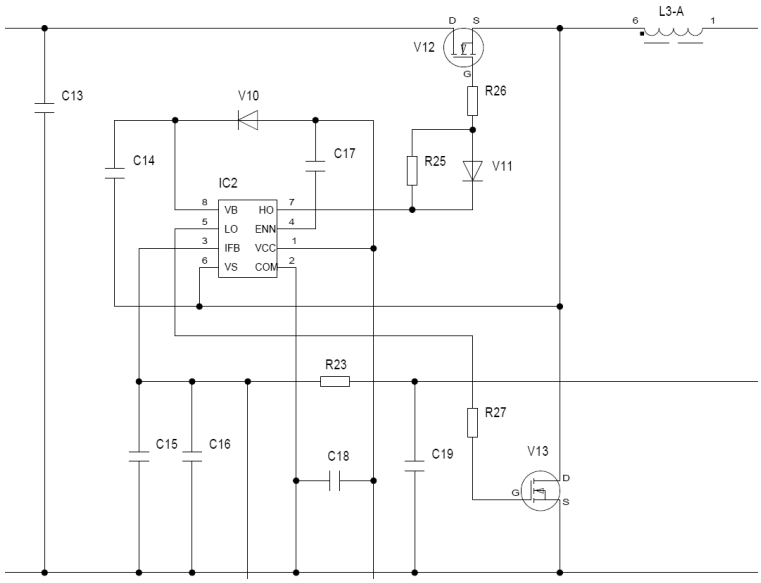


Figure 23. *Buck and control.*

The supply voltage for the buck controller, the PFC controller and for the operational amplifier is pumped from supply via secondary windings of pre-converter and buck chokes.

4.2 Standards

According to the data sheet the LED –driver LL1x23-80-E-CC is in conformity with the following standards:

- EN 61347-1
- EN 61347-2-13
- EN 61000-3-2
- EN 61000-3-3
- EN 55015
- EN 61547
- EN 62384

In this chapter, those standards are introduced under two headings; first General and safety standards and then EMC related standards.

4.2.1 General and safety

The general and safety requirements EN 61347-1 is uniform with IEC 61347-1, Lamp Controlgear Part 1. IEC 61347-1 converses on general and safety requirements and tests, which are considered with most type of lamp controlgear. IEC 61347-1 introduces terms and definitions, general requirements, classification according to the method of installation and items to be marked on the device. It defines demands for protection, electric strength and operating in fault conditions. Creepage distances and clearances are given in Clause 16 and those values needs to be taking account in PCB design. As it is shown in Table 1, creepage distance is defined according to PCB's proof tracking insulation (PTI) and RMS working voltage. Tests according to IEC 61347-1 are type tests. Type tests ensure, that product is compatible with standards and tests are carried out with one sample. [10]

Table 1. *Minimum distances for AC (50/60 Hz) sinusoidal voltages. [10]*

RMS working voltage not exceeding V		50	150	250	500	750	1000
Creepage distance		**Distance [mm]**					
Basic insulation PTI	≥ 600	0.6	0.8	1.5	3	4	5.5
	< 600	1.2	1.6	2.5	5	8	10
Supplementary insulation PTI	≥ 600	-	0.8	1.5	3	4	5.5
	< 600	-	1.6	2.5	5	8	10
Reinforced insulation		-	3.2	5	6	8	11
Clearances							
Basic insulation		0.2	0.8	1.5	3	4	5.5
Supplementary insulation		-	0.8	1.5	3	4	5.5
Reinforced insulation		-	1.6	3	6	8	11

Standard EN 61347-2-13 is practically the same as IEC 61347-2-13, Particular requirements for d.c. or a.c. supplied electronic controlgear for LED modules. The biggest differences between IEC 61347-1 and IEC 61347-2-13 are in abnormal conditions and Annex I, which contains particular additional requirements for independent SELV controlgear for LED modules. Annex I introduces more definitions, classifications and markings. There are also some demands for protection against electric shock, heating, short-circuit and overload. [10; 11]

Performance requirements for electronic control gear for LED modules are introduced in standard IEC 62384 and it is the base of standard EN 62384. IEC 62384 also contains terms and definitions, classification and marking requirements. The tests according this standard are included in type tests. Output voltages and currents during operation, starting and connecting are determined in Clause 7. There are also notes for capacitive load and voltage surges during switching and operation. [12]

4.2.2 EMC related standards

Immunity standard EN 61547 makes only an allusion to IEC standard 61547 where EMC immunity requirements are defined for general lighting purpose equipment. IEC 61547 introduces mainly test specifications. Tests consider electrostatic discharge, radio-frequency electromagnetic and power frequency magnetic fields, fast transients, injected currents and surges. Also tests for voltage fluctuations, dips and short interruptions are specified. This standard aims to ensure that product will work in the real world where interferences occur always. Other EMC related standards consider interferences produced by examined equipment. [13]

Standard EN 61000 is straightly based on IEC 61000, which considers EMC and is published in nine separate parts. Part 3 contains emissions and immunity limits. Part 3-2, Limits for harmonic current emissions, is applicable to equipment having maximum input current 16 A per phase. Defined limits consider systems with at least 220 V nominal voltage. The standard classifies equipment on four classes for harmonic current limitations. Class C contains only lighting equipment. IEC 61000-3-2 determines limits for harmonic currents and introduces measurement circuits and test conditions. Part 3-3 concerns the limitation of voltage changes, voltage fluctuations and flicker in public low voltage systems with current up to and including 16 A per phase. The standard includes assessment of voltage change, voltage fluctuations and flicker, limits and test conditions. [14; 15]

International standard CISPR 15, Limits and methods of measurement of radio disturbance characteristics of electrical lighting and similar equipment, determines limits for insertion losses, disturbance voltages and radiated electromagnetic disturbance. CISPR 15 introduces application of the limits and operation conditions for lighting equipment. Method of measurements for insertion losses, disturbance voltages and radiated electromagnetic disturbance are presented in own clauses from 7 to 9. Clause 10 considers interpretation of CISPR radio disturbance limits. Annex B, Independent method of measurement of radiated disturbance, introduces test set-up for

coupling-decoupling network (CDN) method for conducted RF emission test. This method is used in type tests of Helvar and also in this thesis. [16]

4.3 Main EMC problems and learnings from the previous products

Usually the mechanical specs are determined before PCB design and in some cases before circuit design. That determines the dimensions of the PCB and usually there is no space to be "creative" with placement and segmentation. The most common restrictive feature of Helvar mechanics is that they are long and narrow.

Existing knowledge should be utilized to prevent unnecessary work and waste of time and money. This chapter introduces these known principles following the order in the block diagram shown in Figure 20.

The front part of LED driver corresponds to electronic ballast circuits. Hence, RFI filter, rectifier and PFC principles of layout design can be determined from ballast devices. Usually the term PFC includes also pre-converter. Traces from the supply connector (X1) to first X-capacitor and foil fuse should be as short as possible. Components of RFI filter and rectifier should be placed like one block and naturally traces need to be kept short.

The pre-converter switches high current from the rectifier and hence may cause interference. The connection between the choke, the diode and the MOSFET needs to be short to prevent radiation. Also the snubber circuit loop on MOSFET should be kept small. The choke and FET are hot, hence FET shouldn't be placed right under pre-converter choke and some additional copper should be added to drain, if possible. Components of voltage feedback and feedback compensation should be placed close to PFC-controller and connected to the same ground similarly as other components relating to PFC-controller, except for current feedback resistors. Current feedback resistor must be connected to the high current ground. The ground where high current flows is not allowed to be used as a signal ground, but the PFC-controller ground should be near the ground on which current feedback resistors are connected.

Two most important things with the buck circuit are to keep the buck loop as small as possible and place the buck regulator control near FET or FETs. The most ideal place for the controller is between two controlled MOSFETs. If that isn't possible, traces from and to controller should be still quite short. The filter capacitor connected on current feedback pin of the buck controller needs to be right at the pin. The ground of the controller and components related should be close to high current ground of the buck circuit. But like with the PFC-controller ground, the high return current may not flow via pins of buck controller or related components. FETs become hot and are not allowed to be placed under the electrolytic capacitor(s) since the operating life of the electrolytic capacitor is heavily influenced by the temperature. Adding some extra copper on drains is recommended also with buck MOSFETs.

Obviously, the best place for the controllers isn't right below chokes, and decoupling capacitors should be placed close to supply pins. Components should be nearer to the controller than the amplifier in connections between the buck controller and the operational amplifier. Sensitive traces should be routed away from chokes and ground trace can be used as a guarding ring if necessary.

4.4 Design rules and manufacturability

Design rules contain requirements and recommendations based on electrical principles and standards of course but also on manufacturability. Helvar has its own production and two subcontractors, Plant1and Plant4, for electronic ballasts and LED drivers. Wave soldering is used in all productions. These production plants have their own requirements and PCBs should be optimized for the production plant, where the production is performed. Requirements and recommendations pertain mainly to trace width and clearance, component placement and part models. Some of the products are produced in all three plants and therefore design rules must be harmonized. For the future it would be beneficial to design all PCBs to be suitable for all productions with harmonized rules. Some things, like hole sizes, are never suitable for all three plants, but that isn't a problem since subcontractors can modify that kind of features on their own. If they modify a PCB design, they send files to Helvar for approval.

This chapter introduces the most important rules. Design software CADStar enables defining a set of design rules which can be also checked and at the end of this chapter a collection of harmonized design rules are introduced as an example.

Creepage distance for a PCB, with less than 600 basic insulation PTI, is determined as 2.5 mm according to Table 1. In PCB design this means that clearance between the supply connector pads and traces until the first component that chokes the current, usually the RFI choke, need to be at least 2.5 mm. According to the same table, in SELV products creepage distance and clearance need to be at least 6 mm between isolated parts. This is unconditional requirement. [10]

Obviously trace width depends on trace type. Wider traces are needed in connections where higher currents flow. Minimum trace width is often 0.254 mm but sometimes there is need to use only 0.2032 mm width with signal traces. Plant1 recommends 0.3 mm for minimum trace width and that should be used if it's possible. For example, Table 3 lists trace widths according to net route code used in LL1x23-80-E-CC. CADStar offers automatically the optimal trace width, but designer can choose offered width between limits manually. In practice, the used minimum trace width was 0.3 mm except for foil fuses. The trace code 4 is used for high current and voltage traces from a supply connector to an output connector.

Table 2. *Example of trace widths.*

	Min	Max	Necked	Optimal
4	0.2540	0.6858	0.5080	0.6858
GND	0.2032	0.8890	0.6858	0.8890
SIGNAL	0.2032	0.6858	0.2540	0.3048
VCC	0.2540	1.0160	0.2540	1.0160

The protective ground needs very wide trace, 2 mm at least, and it is easiest to produce with copper area. Also ground trace from Y-capacitor to the diode bridge and the ferrite L5 should be kept as wide as possible. Broadly, it is justified to use large copper areas rather than just traces in supply, diode bridge and main circuits of pre-converter and buck. Another specific trace width is in foil fuses, which are determined to be 0.254 mm wide and 5.5 mm long.

Both subcontractors have defined component placement orientation to be perpendicular to soldering direction and 0402 as minimum SMD component size. Plant1 has determined minimum distance from components to board edge and between components more precisely than Plant4. Minimum distances between components are defined by Plant1 and they are presented closely in Table 4.

Table 3. *Minimum distance between components.*

Package size	Height [mm]	Distance [mm]
0603	≤ 1	0,8
	1 <	0,8
0805	≤ 1	0,8
	1 <	1
1206	≤ 1	1
	1 <	1,2

Plant1 recommends minimum distance from board edge to components to be 1 mm and at the end of the board at 3 mm. Plant4 has suggested 5 mm minimum distance from board edge for cheaper PCBs, but that is impossible with almost every product.

The distance is important especially with big ceramic capacitors, because they crack easily if they are too close to the board edge. Also recommended minimum distance between SMD pad and PTH pad is 1 mm. Helvar's own production requires 2 mm minimum distance between passive SMD components and ICs or other big components at soldering direction.

The minimum length of PTH component is 12.5 mm for Plant4. Plant1 is more specific and requires for PTH components from body length plus 5 mm to 20 mm length with 2.5 mm steps. PTH diodes might break, if leads are bent too close from the body and the recommended raster for diodes is 12.5 mm. The length of jumper starts at 6 or 7 mm and the step is 2.5 mm and for jumpers shorter than 20 mm the diameter of 0.6 mm is enough. For over 20 mm long jumpers required diameter is 0.8 mm. The lengths of PTH components are listed in Table 4. As explained in the chapter 3.5, lead lengths should be retained short remembering limitations. The minimum distance between two jumpers must be 2.05 mm but 2.25 mm would be better. The isthmus between two holes under 3 mm diameter should be at least 0.75 times board thickness which is 1.2 mm on 1.6 mm board. On one-sided board Plant1 requires 0.4 mm bigger pad diameter than the hole size. Helvar's production recommends 0.4 mm neck for PTH pads and the minimum is 0.35 mm.

Table 4. *Required lengths for PTH components.*

		Minimum length [mm]	Step [mm]	Maximum length [mm]
Plant4	PTH component	12.5		
Plant1	PTH component	body + 5	2.5	body + 20
Plant1	Jumper 0.6 diameter	6 / 7	2.5	20
Plant1	Jumper 0.8 diameter	20	2.5	

In controllable products, test points are needed at least for a microprocessor. The placements of test points are predefined, if production has suitable test equipments already. If new tester is needed anyway, for example for a new product family, designer can determine places for test points. Plant1 requires 1.5 mm minimum distance between two test points and 0.7 mm from solder joint. In Helvar's own production a test point is 1.7 x 1.7 mm square and the minimum distance between centers of test points is 2.7 mm.

An example of design rules to fill on CADStar's design rules is introduced in Table 5, where minimum distances are in millimeters. These rules are harmonized to be suitable for every production and can be modified for example according to specific plant.

***Table 5**. An example of used design rules in CADSTAR Design Editor 13.0.Distances are in millimeters.*

Comp Placement to Comp Placement	1.000	Route to Board	0.500
		Route to Copper	0.300
Copper to Board	0.500	Route to Pad	0.300
Copper to Copper	0.300	Route to Route	0.300
		Route to SMD Pad	0.300
Hole to Hole (< 3mm)	1.200	Route to Via	0.300
Pad to Board	1.000	Test Land to Board	0.5000
Pad to Copper	0.300	Test Land to Component	1.000
Pad to Pad	1.000	Test Land to Test Land	1.500
Pad to SMD Pad	1.000		
Pad to Via	0.300	Via to Board	0.5000
		Via to Copper	0.300
SMD Pad to Board	1.000	Via to SMD Pad	0.300
SMD Pad to Copper	0.300	Via to Via	0.300
SMD Pad to SMD Pad	1.000		

Also some specific component patterns and hole sizes for productions exist, mostly for Plant1, but those are usually suitable also for Plant4 and for Helvar's own production. Hole sizes depend on whether they are placed by hand or by machine and that depends on line where a product is made.

4.5 PCB Designs for experiments

The production PCB for LL1x23-80-E-CC is tried to optimize on every aspect. The PCB design of the second prototype, which is used as reference board, is illustrated below in Figure 24. The target in this thesis is to investigate effects of some design solutions and principles: do they have an effect, and if so, how significant. According to results it may be found which principles are the most important to be optimized and is there some things that don't have an effect at all.

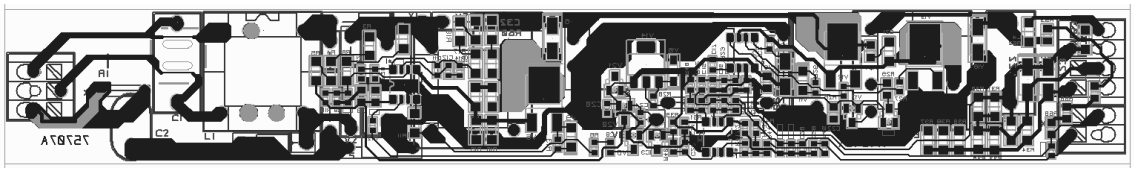


***Figure 24.** LL1x23-80-E-CC production PCB 75707A design with component, bottom copper and bottom solder resist photo layers.*

Modified details were chosen on the basis that it can be implemented in practice. In each test PCB just one detail was modified and other differences on every PCB have

been tried to keep minimal. If a PCB changes too much, it would be impossible to know which change causes which result.

Every PCB design guide recommends to use as wide ground traces and coppers as possible. It is interesting to see whether it has any effect on EMI. If not, designer won't need to arrange extra copper for the ground. In the first PCB, DIA1, the high current ground trace is just 0.8890 mm width, which is the minimum on the production version 75707A. Component placement is exactly the same as on 75707A. The difference in copper layers is shown in next Figure 25 with pink, the 75707A copper layer is the upper.

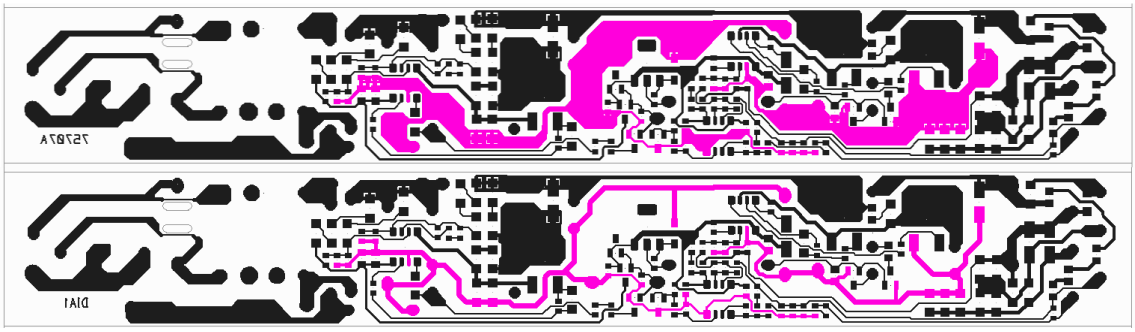


Figure 25. *Difference between bottom copper layers of 75707A (upper) and DIA1 (lower).*

The first thing that pops up when Helvar's older PCBs are explored is that the high current ground is on the opposite edge of the board than the high current and voltage trace. The loop of high current seems to be unfavorably big. Later the ground is intended to get closer to the high voltage trace. The purpose of DIA2 is to find out how significant impact the location of the ground has. If difference is negligible, designers don't have to consider how to get the ground close to the high voltage trace.

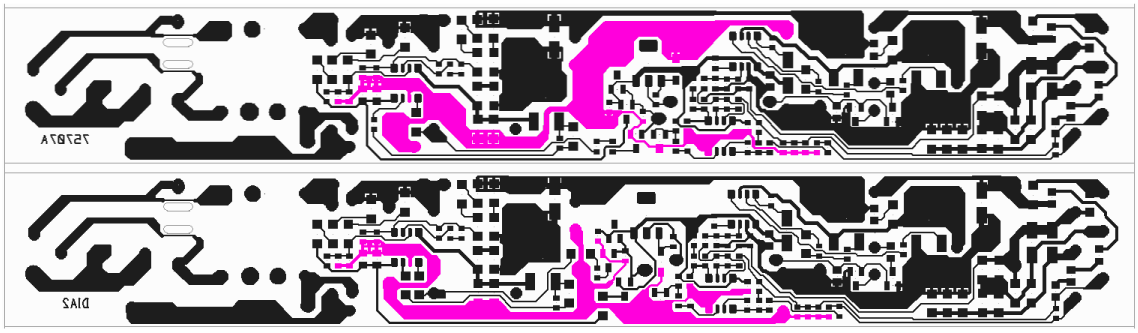


Figure 26. *Differences on ground locations on bottom copper layer.*

Figure 26 shows the difference between groundings. Some component placements needed to be changed slightly, which included changes in associated traces. The jumper in high current grounding remains on test board DIA2 but it is shorter as can be seen on Figure 27.

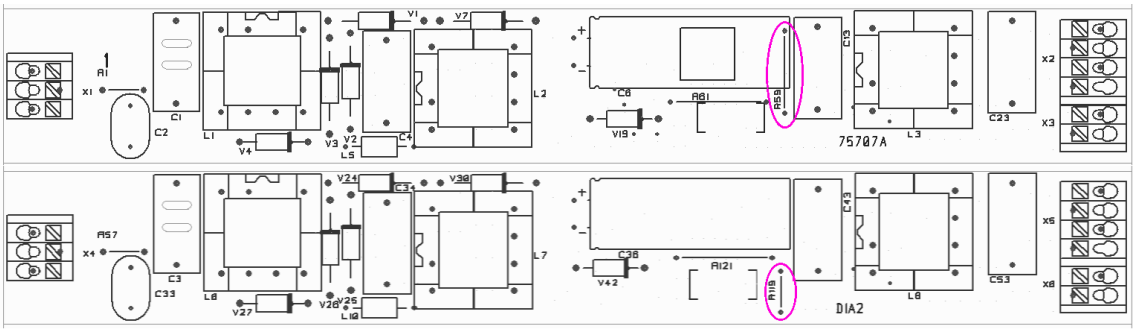


Figure 27. *The difference between ground jumpers on top silk layer.*

Buck loop and buck control is examined with the third PCB, DIA3. In Figure 28 is presented differences between the buck circuits of 75707A (above) and DIA3, where buck capacitors, FETs and control IC are highlighted. On production PCB 75707A the buck capacitor is right next to MOSFET V12 and hence the buck loop is small. The disadvantage of this arrangement is that the control, IC2 and related components, is quite far away from FETs to control. Specifically, signal trace from IC2 to FET V13 is long. On DIA3 the control is placed between FETs and signal traces to FETS are shorter, but the buck loop is bigger. The purpose of DIA3 is to investigate which is more significant, the size of the buck loop or lengths of the control traces.

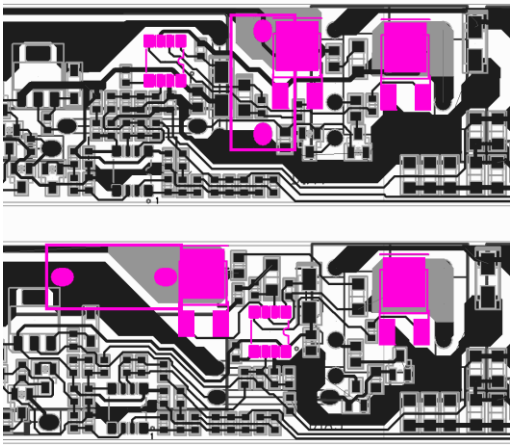


Figure 28. *Differences between buck circuit and placements of ICs. Visible layers are component placement on both layers, bottom copper and bottom resist photo.*

Pre-converter current is measured by two resistors for PFC. Traditionally in Helvar's PCBs these resistors are placed near the PFC-controller and grounded on the ground pin of the electrolytic capacitor. The other possibility is to ground these measurement resistors on the ground pin of the X2-capacitor. On DIA4 resistors for current measurement are grounded to the X2 capacitor. In Figure 29 is current measurement resistors, X2-capacitor, electrolytic capacitor and ground pins of those components are highlighted.

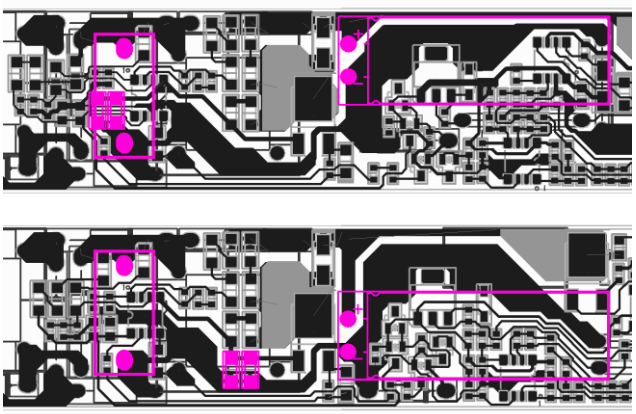
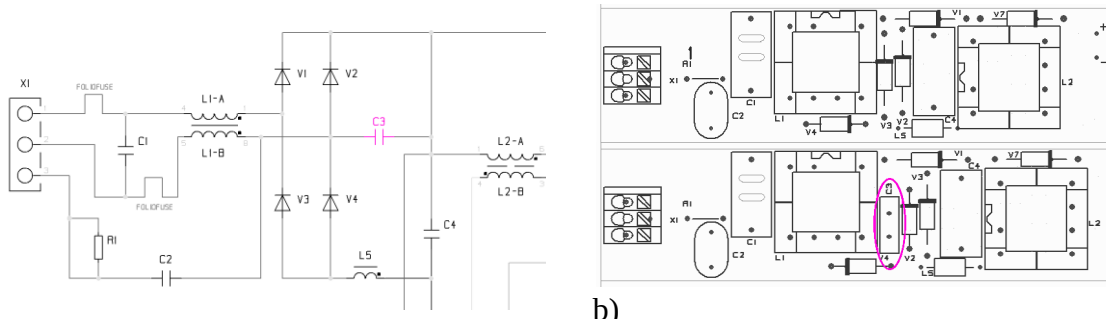


Figure 29. *Different placements for current measurement resistors.*

In the RFI filter, the Y-capacitor can be connected on RFI-choke instead of diodes if a capacitor is added. One leg of the additional capacitor is connected to the Y-capacitor, the choke and between two diodes and the other leg is connected to the output of the diode bridge, the X2-capacitor and the pre-converter choke. The connection is presented in Figure 30 a) and the added capacitor on the board DIB5 in Figure 30 b).



a) b)

Figure 30. *a) Additional capacitor C3 in schematic. b) The placement of additional capacitor C3 on top silk layer (lower) corresponded to top silk layer of 75707A.*

The ground connection from Y-capacitor to the diode bridge and the ferrite is usually as wide as possible. The purpose of PCB DIB6 is to test what happens if the trace is narrow, only 0.8890 mm. The difference is shown in Figure 31 below.

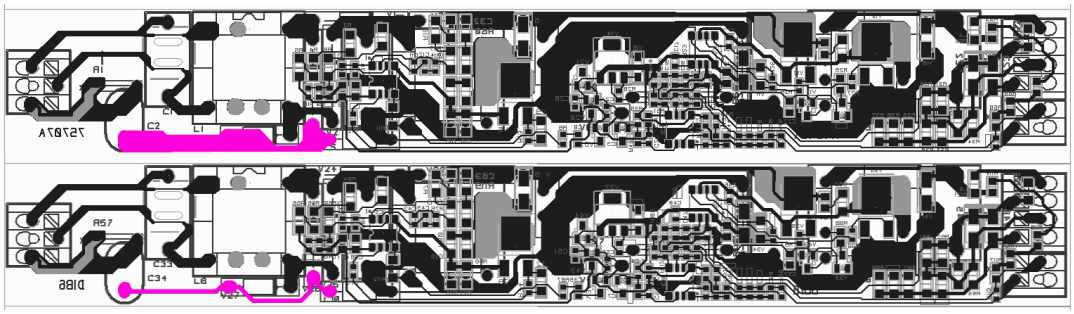


Figure 31. *Narrow trace from the Y-capacitor. Visible layers are component placement on both layers, bottom copper and bottom resist photo.*

In 75707A the X2 capacitor is grounded just next to the leaded ferrite bead inductor. As can be seen in Figure 32, in test board DIB7 the ground pin of X2 capacitor is slightly apart from ferrite at the end of quite narrow trace and high current won't flow smoothly through that pin.

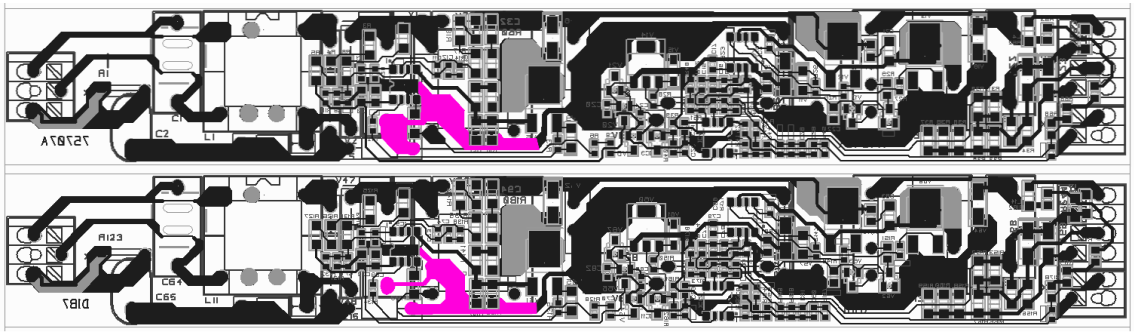


Figure 32. *Difference between X2 capacitors groundings. Visible layers are component placement on both layers, bottom copper and bottom resist photo.*

On 75707A traces from supply connector to the first X-capacitor are as short as they can be. Sometimes those traces aren't so well optimized. With the last test PCB, DIB8, the purpose is to determine how essential it is to minimize the length of these traces. Figure 33 highlights the supply traces on the production PCB and on the test board.

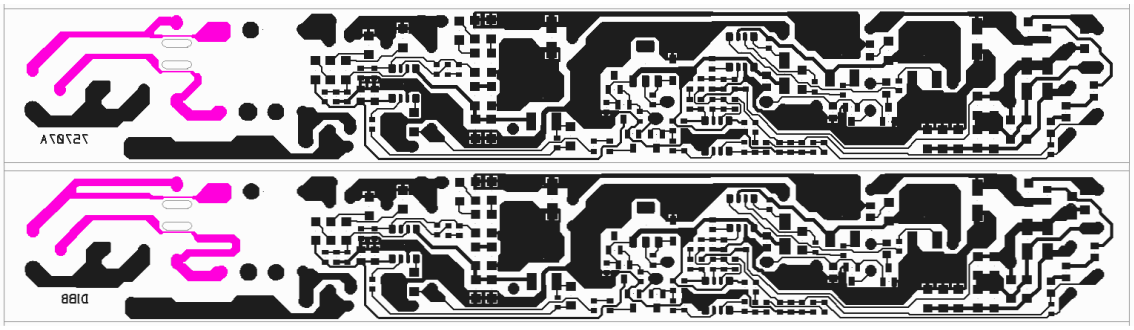


Figure 33. *Supply traces from connector to RFI-choke on bottom copper layer.*

In this chapter figures illustrate only differences between PCBs and the whole PCB designs are represented in Appendix A. PCBs were designed and ordered in two panels, DIA and DIB. The panel DIA contained PCBs DIA1 – DIA4 and the panel DIB contained PCBs DIB5 - DIB8. Appendix A represents PCB designs in the panel layer by layer. Layers of panel are shown in Figures A.1 - A.5 in the order of drill drawing, top silk, bottom silk, bottom copper and bottom solder resist. Layers of panel B are presented in the same order in Figures A.6 – A.10.

5 MEASUREMENTS

Functionality of every PCB, including the reference 75707A, was verified with a resistor load and an oscilloscope before RFI measurements. Some of the PCBs were reworked because of wrongly assembled diodes or wrong size resistors.

5.1 Measurement procedures

The measurements in this thesis are performed using the same RFI measurement equipment and test chamber, which are normally used at Helvar for type testing. The walls and the roof of the RFI-chamber are built of metal net. Also the door is made of metal. Figure 34 is taken outside of the test area.

a) b)

Figure 34. *The RFI test chamber from outside.*

Normal type tests are measured with 230 VAC and 240 VDC supplies and with all permitted loads, since several different loads can be allowed, like in the case of LL1x23-80-E-CC. The measurements were performed according to typical type test, but with only one load and 230 VAC supply voltage. Since the radiated disturbances are most significant with high output current, the selected load was the highest possible 350 mA and 228 V.

Both conducted and radiated emissions are measured in three different situations: with ground, without ground on a metal plate and without ground on a wooden board.

With ground, the purpose is to simulate a situation in which the driver is located in a Class I luminaire. Class I luminaire is always grounded and also its metal body is also grounded. This situation is simulated by placing the driver board on a grounded metal plate and by grounding the driver board. The measurement with the metal plate and without grounding represents a situation in which the driver is placed in a Class II luminaire with metal body and live parts are double or reinforce insulated. Class II luminaire body can also be made of plastic. The wooden board without ground simulates plastic Class II luminaire without ground connection and independent use. Luminaires are classified according to the electrical shock protection type and classifications are defined in standard IEC 60598-1 in definitions 1.2.20-1.2.24. [17]

5.1.1 Radiated emission measurements

Radiated emission is measured with CDN-method (coupling-decoupling network) according to standard CISPR 15. In CDN-method for radiated emission, the measured signal is actually conducted emission, but it reflects on radiated emission and the used frequency range is from 30 MHz to 300 MHz. The measurement device is Teseq's M-type coupling-decoupling network. With M-type, cables from the CDN are connected to equipment under test (EUT). Figure 35 shows the principle of test set-up for CDN-method according to CISPR15.

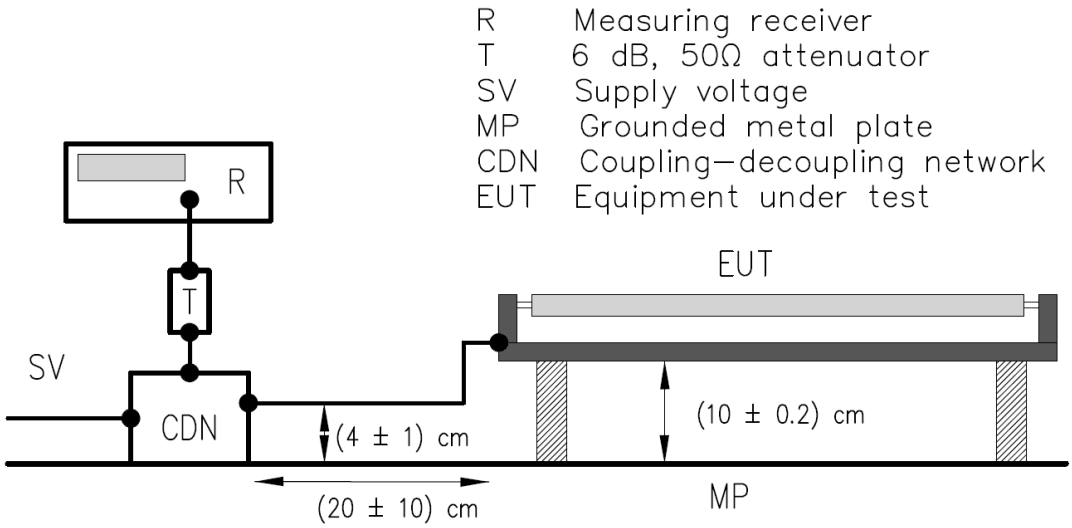


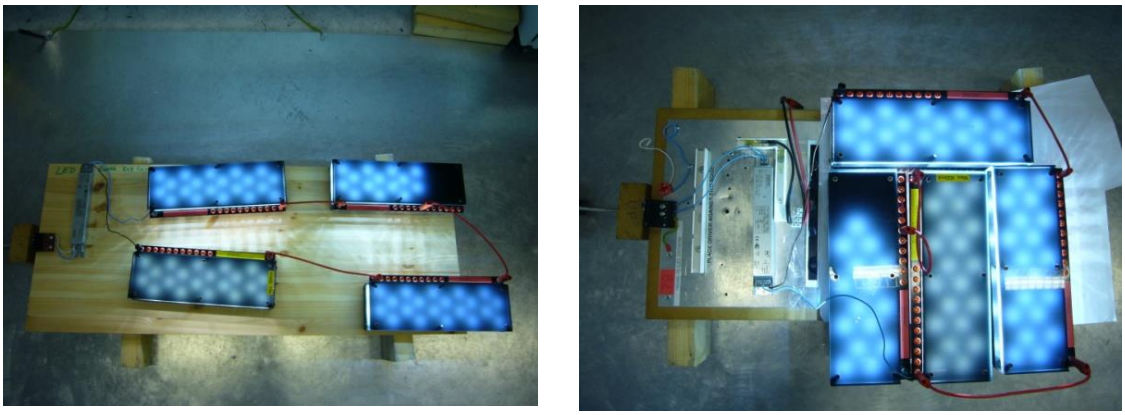
Figure 35. *Test set-up according to CISPR 15 CDN method.[16]*

Because radiated emission is measured with and without ground, two CDN-devices are needed. Without ground the measurement device is M2 type and with ground M3. The connector of CDN M2 has wires for line (L) and neutral (N), which can be seen in Figure 36 a). CDN M3 connects also the board to safety ground, as can be seen in Figure 36 b). Also the grounded metal plate and a wooden brick for setting wires in right direction and distance from the metal plate are shown in Figure 36.

a) b)

Figure 36. *CDN connection to board a) without ground with M2 and b) with ground and M3.*

The 228 V load is constructed of four LED modules which are connected to each other with wires. Test setup on wooden board is shown in Figure 37 a) and on metal board in 37 b). Figure 37 b) also shows some paper sheets under LED loads which isolates load when the metal plate is isolated. Wire placement effect the radiated emission measurement results. If test setup changes between measurements, results can't be compared to each other. Hence wires are taped to the board and test setup is kept the same until all PCBs are measured to minimize setup changes.



a) b)

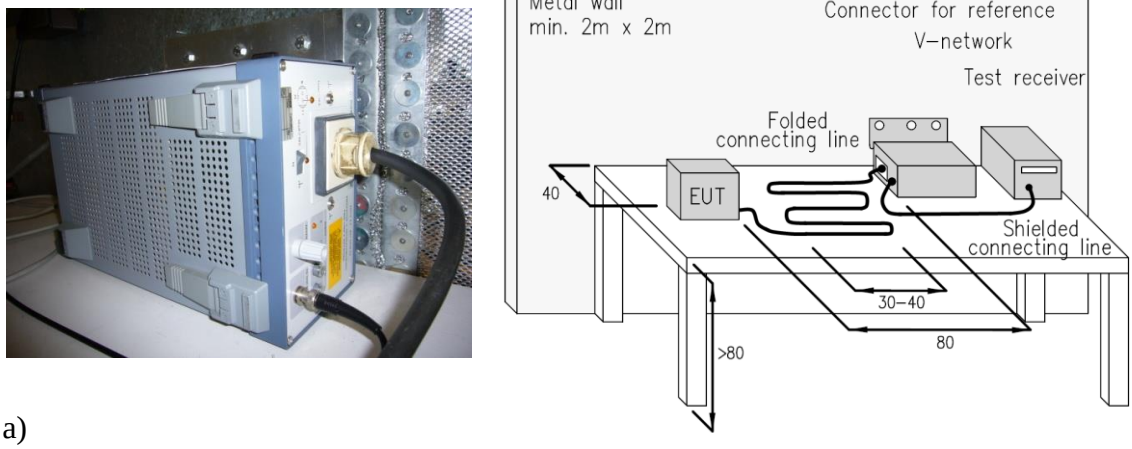
Figure 37. *Test setup on a) wooden board and b) metal board.*

After all PCBs are measured the test set up is changed to other. Radiated emission measurements are done for every test PCB, DIA1-4 and DIB5-8, and reference PCB 75707A.

5.1.2 Conducted emission measurement

Conducted emission measurements are performed with the artificial mains network (AMN). Used AMN Rohde & Swartz's Two Line V-network ESH3-Z5 is shown in Figure 38 a) [18]. ESH3-Z5 is suitable for measurements both with and without ground

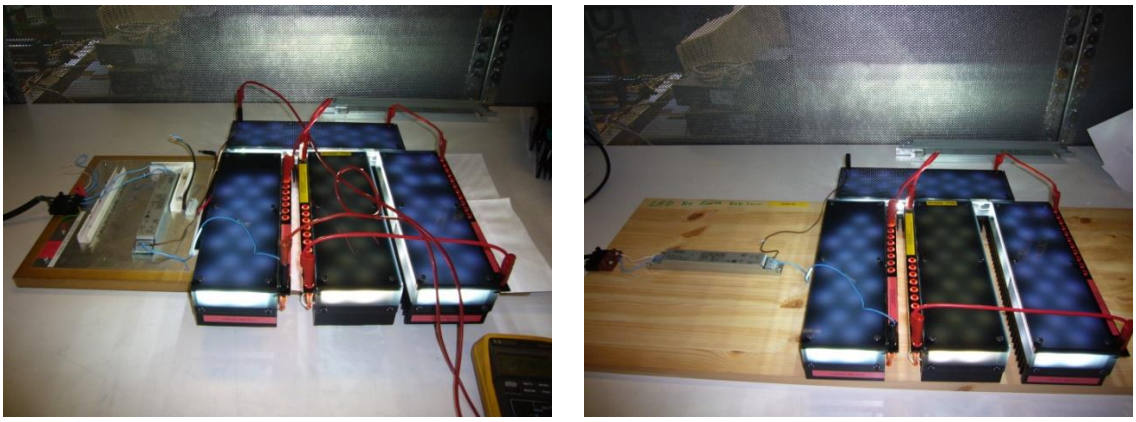
just by changing the cable. The difference between the cables is that the cable for measurements with ground has the wire for safety ground. Used frequency range for conducted emission is from 9 kHz to 30 MHz. The test setup with demanded dimensions is introduced in Figure 38 b).



a) b)

***Figure* 38.** *a) Artificial means network ESH3-Z5. b) Test setup for conducted emission.[18]*

Test boards are the same as for radiated emission measurements and test setups are shown in Figure 39. Although the placement of wires is not so crucial in the case of conductive emission, the wires between the load and the driver are still taped to the board. Before starting measurements LED loads are pre-heated because threshold voltage of LED loads drops a few volts when LEDs are heated. The Figure 39 a) is a photograph taken during LED loads pre-heating and the multimeter is also shown. Pre-heating was also performed before radiated emission measurements. Every driver was also pre-heated for about five minutes before starting measurements.



a) b)

Figure 39. *Test setup for conducted emission on a) metal board and b) wooden board.*

The PCB won't affect as much on conducted emission as the circuit design and component choices. Hence conductive emission measurements are performed only for the reference PCB 75707A and for DIB5 where the RFI filter differs from the reference.

In both radiated and conducted emission measurements the receiver is R&S ESPI EMI Test Receiver. [19] The receiver is placed outside of the RFI-measurement area and it is connected to normal PC. Measurements are operated via ES-Scan software. First, settings need to be chosen from predefined settings according to test type and equipment. The system measures first peak values of emissions roughly over the frequency range. When the pre-measurement is complete, the system measures more precisely those frequencies where the disturbance exceeds 9 dB margin. Helvar requires 5 dB margins in final measurements to ensure that the drivers are suitable for all luminaires. These values are quasi peak values. If pre-measurement is below the margin in whole frequency range, the precise measurements are not performed. The results can be printed after every measurement on paper or in PDF-file.

5.2 Results and discussion

EMI Measurement Test Report shows results of one measurement in two parts. The pre-measurement graph is shown in the first slide and the second slide shows the final measurement table. In graph of radiated emission, CISPR15Q limit is drawn in red and pre-measurement in blue. Final measurement results show the magnitude of interference at precise frequencies and the frequencies vary with every PCB. Final results are marked also in the pre-measurement graph with red triangulars.

Two limits and two pre-measurements are drawn in a pre-measurement graph of conducted emission. Limits are according to EN55015. Quasi peak limit is drawn in red and average limit is in pink. Measured peaks are blue and average value is green. Final measurement results are marked with red triangles as in the case of radiated emission.

In this chapter the results are presented in Figures 40 – 43. Every figure represents pre-measurement result for all PCBs in the test setup with some most significant margins. Full results can be seen in Appendix B. Table 7 shows in which figure pre-measurement result and in which table final measurement results can be found for each PCB. The final column of the table shows the measurement type; Radiated or Conducted. Also the changes done in PCBs are summarized in Table 7.

Table 6. *Summary of PCB's differences and test results in Appendix B.*

		Appendix B				
		Figure			**Table**	
PCB	**The change**	**Ground**	**Metal**	**Wood**	**Final**	R/C
75707A	Reference PCB	B.1. a)	B.1. b)	B.1. c)	B.1.	R
		B.2. a)	B.2. c)	B.2. e)	B.2.	C
DIA1	Narrow ground trace	B.3. a)	B.3. b)	B.3. c)	B.3.	R
DIA2	High current ground at the other side of the PCB	B.4. a)	B.4. b)	B.4. c)	B.4.	R
DIA3	The buck loop and control	B.5. a)	B.5. b)	B.5. c)	B.5.	R
DIA4	Current measurement resistors	B.6. a)	B.6. b)	B.6. c)	B.6.	R
DIB5	Different Y-capacitor connection and the additional capacitor	B.7. a)	B.7. b)	B.7. c)	B.7.	R
		B.8. b)	B.8. d)	B.8. e)	B.8.	C
DIB6	Narrow ground trace from the Y-capacitor	B.9. a)	B.9. b)	B.9. c)	B.9.	R
DIB7	Not so good grounding for X-capacitor	B.10. a)	B.10. b)	B.10. c)	B.10.	R
DIB8	Longer supply traces between connector and X-capacitor	B.11. a)	B.11. b)	B.11. c)	B.11.	R

Measurement results are introduced in the order of test setup; first radiated emissions with ground on the metal plate, without ground on the metal plate and without ground on the wooden board. Lastly, conducted emissions measured from 75707A and DIB5 are represented.

5.2.1 Results of radiated emissions with ground

Pre-measurement results of radiated emission on the metal plate with ground for all PCBs are presented in Figure 40. Values of smallest margins from final measurements are also marked in Figure 40 for frequency ranges 30 – 50 MHz, 50 – 70 MHZ, 70 – 100 MHz and 100 – 300 MHz. Margins with smallest values are underlined.

The reference board 75707A passed measurement clearly with ground on the metal plate. Interferences were more than 9 dB below limit and therefore no final measurements were done, as it is shown in figures 40 a) and B.1. a).

Figures 40 a) and b) show that results of DIA1 were remarkably worse than 75707A. Final measurements were taken at eight frequencies although all of them were below the 5 dB margin as can be seen in Table B.3. The smallest margin was 7.31dB at frequency around 60 MHz as is shown in Figure 40 b). According to figures B.3 a) and B.1 a), interferences of DIA1 were higher than in 75707A up to 70 MHz.

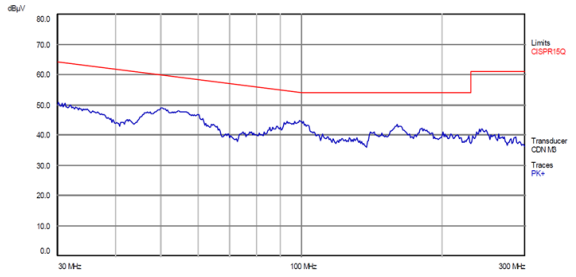
As can be seen from Figure 40 a), b) and c), results of DIA2 were worse than 75707A, but not as significantly as DIA1. According to Table B.4 and Figure B.3 a), with ground there were no overdrafts and all final measurements were below the 5 dB margin. As marked in Figure 40 c), the narrowest margin was 11.33 dB and as Figures 40 a) and c) show, interferences of DIA2 were constantly slightly bigger than with 75707A at frequencies under 70 MHz.

DIA3 was slightly worse than 75707A. From Figures 40 a) and d) can be seen, margins were smaller at frequencies below 70 MHz than with 75707A. According to Table B.5 and Figure B.5 a), measured interferences stayed under 5 dB margin in whole frequency range. Increased interference produced by buck can be seen around 60 MHz, but the smallest margin 12.30 dB was measured at frequency below 200 MHz as can be seen in Figure 40 d).

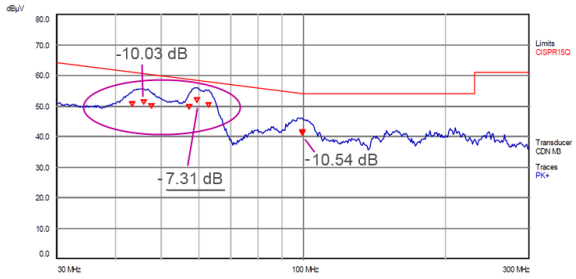
Figures 40 a) and e) show that interferences were significantly higher in DIA4 than in 75707A at frequencies up to 65 MHz. According to Table B.6 and Figure B.6 a), five final measurements were taken at frequencies between 40 MHz to 60 MHz, but all were more than 10 dB below limits. As marked in Figure 40 e), the smallest margin was 10.48 dB at frequency around 50 MHz.

Similarly as 75707A, DIB5 passed measurement without final measurements as it is shown in B.7 a). As shown in Figures 40 a) and f), interferences were lower than they were with 75707A at frequencies below 50 MHz, but just around 60 MHz it was about 5 dB higher.

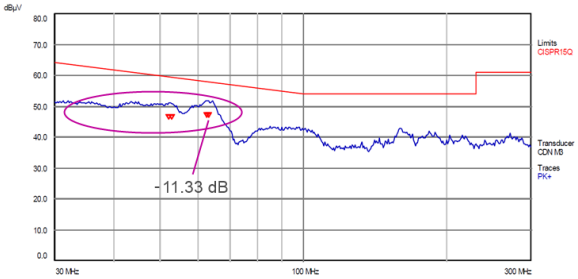
According to Figures a) and g), pre-measured interferences from DIB6 were slightly higher than measured from 75707A at frequencies below 65 MHz. According to Table 9 and Figure B.9 a), all final measurements were way below 5 dB margin. As underlined in Figure 40 g) the narrowest measured margin was 12.93 dB at frequency around 60 MHz.



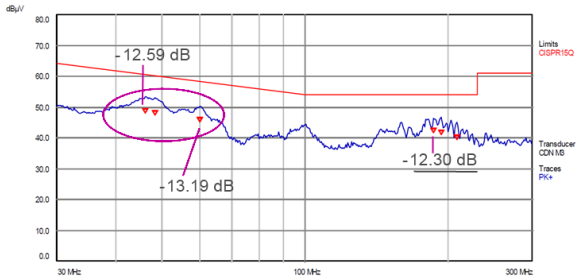
a) 75707A



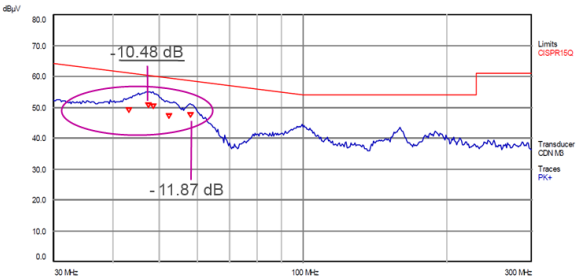
b) DIA1



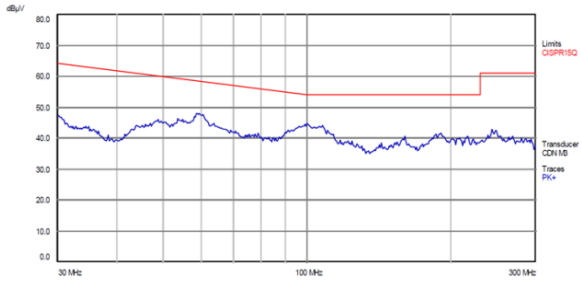
c) DIA2



d) DIA3

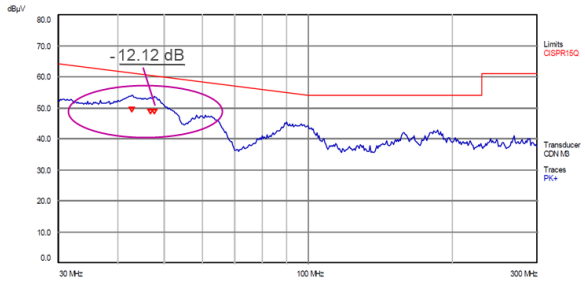


e) DIA4

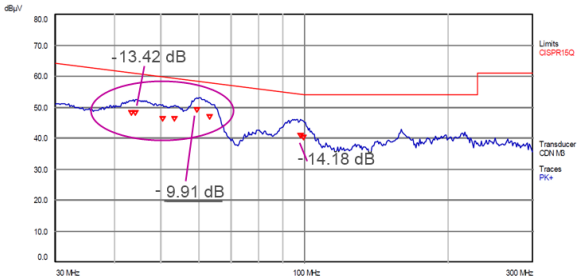


f) DIB5

g) DIB6



h) DIB7



i) DIB8

Figure 40. *Radiated emission pre-measurement results on the metal plate with ground.*

Figures 40 a) and h) show that DIB7 was almost as good as 75707A. Only at frequencies below 50 MHz interference level was slightly higher and according to Table B.10 and Figure B.10 a), measured levels were about 12 dB below limits.

According to Table B.11 and Figures B.1 a) and B.11 a), measured margins of DIB8 were clearly over the 5 dB, though result was not as good as with 75707A, which had no final measurements. Figures 40 a) and i) show that especially at frequencies between 40 MHz to 45 MHZ and around 60 MHz interferences appeared to be higher. The narrowest margin 9.91 dB was measured at 60 MHz as shown in Figure 40 i).

Quantity of final measurements and narrowest margins with measurement frequency are listed in Table 7 according to tables of Appendix B.

Table 7. *Comparison of results on the metal plate with ground.*

PCB	Final Measurement [pcs.]	Narrowest margin [dB]	Frequency [MHz]
75707	0		
DIA1	8	7.31	59.44
DIA2	4	11.33	63.2
DIA3	6	12.3	186.64
DIA4	5	10.48	47.52
DIB5	0		
DIB6	6	12.93	61.28
DIB7	4	12.12	47.6
DIB8	8	9.91	59.6

With ground all other PCBs than DIB5 had higher interferences in pre-measurements when compared to reference PCB 7507A. Specially, at frequencies between 40 MHz and 50 MHz and around 60 MHz differences were significant. Also DIB5 had higher level at 60 MHZ compared to 75707A. DIA1, DIA3 and DIB8 had most final measurements and lowest margins were measured from DIA1. According to pre-measurement graphs and final measurements, DIA1 had worst results.

5.2.2 Results of radiated emissions on the metal plate

Pre-measurement results of radiated emission on the metal plate without ground for all PCBs are presented in Figure 41. Also in Figure 41, smallest margins from final measurements are also marked for frequency ranges 30 – 50 MHz, 50 – 70 MHZ, 70 – 100 MHz and 100 – 300 MHz. Margins with smallest values are underlined.

The pre-measurement of 75707A exceeded the 9 dB margin and final measurements were done as can be seen in Figure B.1 b). According to Table B.1, all final measurements were more than 5 dB below limits. The smallest margin measured was 9.99 dB at 140 MHz as is shown in Figure 41 a).

Figures 41 a) and b) show that measured interferences of DIA1were significantly higher than with 75707A at frequencies below 70 MHz. According to Table B.3 and Figure B.3 b), measurements for DIA1 didn't overdraft limits, but at frequencies between 57 MHz and 63.00 MHz three measured margins were smaller than 5 dB. As marked in Figure 41 b), the smallest margin was only 2.11 dB.

As can be seen in Figures 41 a) and c), interferences of DIA2 were slightly higher than with 75707A up to 70 MHz. According to Table B.4 and Figure B.4 b), there were no overdrafts. The smallest measured margin was 5.33 dB at frequency around 60 MHz as shown in Figure 41 c).

Measurement results of DIA3 are shown in Figure 40 d) and were worse than results of 75707A in Figure 41 a). According to Table B5, all measured margins were bigger than 5 dB. Increased interference produced by buck can be seen in Figures 41 d) and B.5 b), around 60 MHz and the smallest measured margin was 6.40 dB at around 60 MHz.

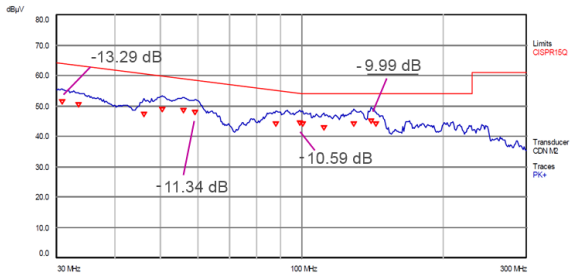
According to Table B.6 and Figure B.6 b), all interferences measured from DIA4 were below the 5 dB margin, but as can be seen from Figures 41 a) and e), margins were significantly narrower than were measured from 75707A frequencies between 35 and 70 MHz. The smallest margin in final measurement was 5.22 dB at frequency around 60 MHz and it is marked in Figure 41 e).

As can be seen from Figure 41 a) and f), measured interferences of DIB5 were significantly lower than 75707A up to 50 MHz, but between 60 MHz to 110 MHz interferences were higher. According to Table B.7 and Figure B.7 b), in final measurements margins were sufficient at whole frequency range. As marked in Figure 41f), the smallest margin, 7.63 dB, was measured around 60 MHz.

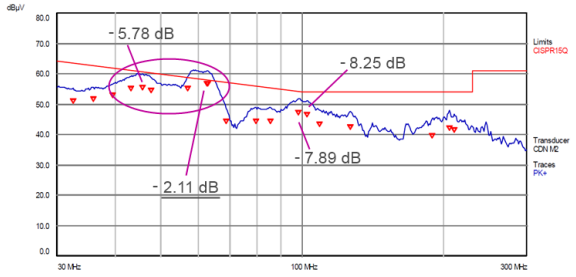
Most significant differences between DIB6 and 75707A were at frequencies between 40 MHz and 50 MHZ and around 60 MHz as can be seen in Figure 41 a) and g). According to Table B.9 and Figure B.9 b), all measured margins were bigger than 5 dB. The smallest margin was 6.08 dB and was measured at frequency 60 MHz as shown in Figure 41. g).

Figures 41 a) and h) show that interferences measured from DIB7 were higher up to 65 MHz than measured from 75707A. According to Table B.10 and Figure B.10 b), all measured margins were sufficient at whole frequency range. As can be seen in Figure 41 h), the smallest margin was 7.47 dB at frequency around 60 MHz.

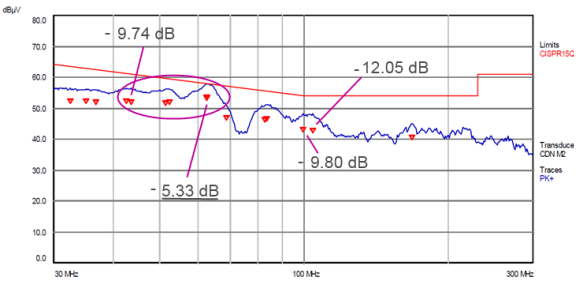
As shown in Figures 41 b) and i), the results of DIB8 were almost as worse than results of DIA1. As Figures 41 a) and i) show that measured interferences were higher than interferences of 75707A at frequencies just between 40 MHz and 50 MHz, and around 60 MHZ. According to Table B.11 and Figure B.11 b), two margins smaller than 5 dB was measured. The smallest margin was 4.05 dB at frequency 62.9 MHz. Only DIA1 and DIB8 didn't reach the 5 dB margin at the whole frequency range as can be seen from Figure 41.



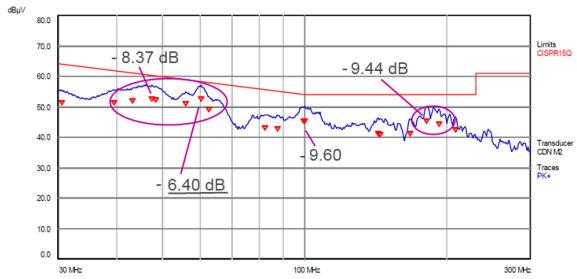
a) 75707A



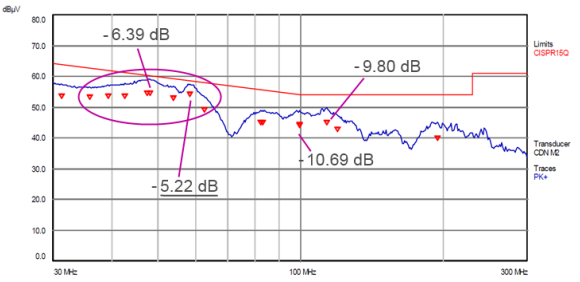
b) DIA1



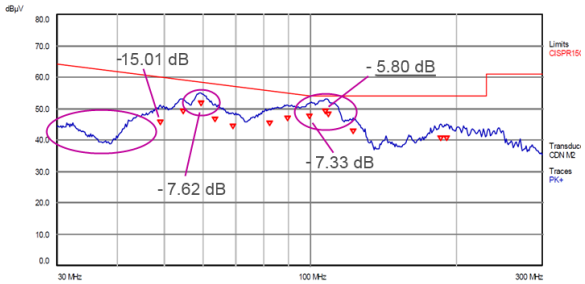
c) DIA2



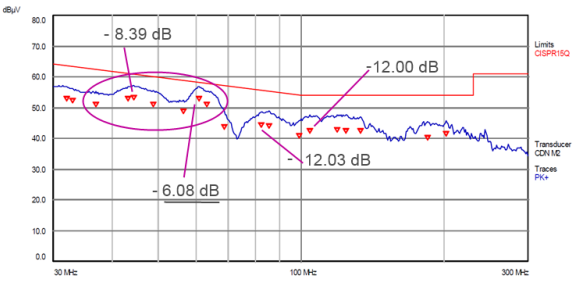
d) DIA3



e) DIA4

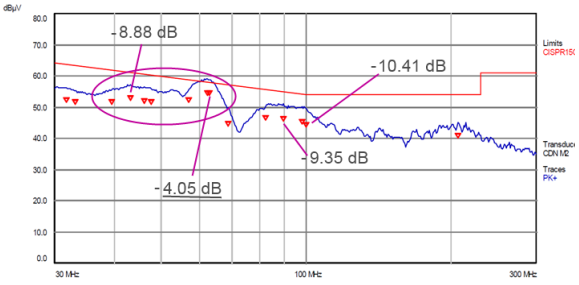


f) DIB5



g) DIB6

h) DIB7



i) DIB8

Figure 41. *Radiated emission pre-measurement results on the metal plate without ground.*

According to tables of Appendix B, narrowest margins are listed in Table 8 for comparison of final measurements. On the metal plate without ground, interferences were higher than in 75707Aat frequencies below 70 MHz on all test PCBs. DIB5 was the exception, on which interferences were much lower at frequencies up to 50 MHz than in 75707A. Only DIA1 and DIB8 didn't reach the 5 dB margin at whole frequency range. The finest measured margin of DIA1 was 2.11 dB at frequency 63 MHz and at almost the same frequency 62.9 MHz was measured the smallest margin of DIB8, 4.05 dB.

Table 8. *Comparison of results on the metal plate without ground.*

PCB	Final Measurement [pcs.]	Narrowest margin [dB]	Frequency [MHz]	Margins < 5dB [pcs.]
75707A	15	9.99	140.6	
DIA1	19	2.11	63.0	3
DIA2	15	5.33	62.72	
DIA3	18	6.4	60.4	
DIA4	16	5.22	58.24	
DIB5	13	7.62	59.6	
DIB6	19	6.08	60.88	
DIB7	16	7.47	61.56	
DIB8	15	4.05	62.92	2

Overall, all test PCBs were worse than reference PCB. DIA1 and DIB8 can be considered as worst with smaller than 5 dB margins and DIA3 and DIA4 second worse, because less than 6 dB margins were measured from both.

5.2.3 Results of radiated emissions on the wooden board

Pre-measurement results of radiated emission on the metal plate with ground for all PCBs are presented in Figure 42. Values of smallest margins or highest overdrafts from final measurements for frequency ranges 30 – 50 MHz, 50 – 70 MHZ, 70 – 100 MHz and 100 – 300 MHz are also marked in Figure 42. The highest overdraft for the PCB is underlined.

Pre-measurement of 75707A in Figure B.1 c) shows, that there were four overdrafts at frequencies between 40 MHz and 55 MHz. The highest overdraft was 1.5 dB at 50 MHz as marked in Figure 42 a). According to Table B.1, eight margins smaller than 5 dB were measured.

Pre-measurement result for DIA1 is shown in Figure 42 b) and in Figure B.3 c). As can be seen in Figures 42 a) and b), the significant difference was around 60 MHz, where DIA1 had two over 2 dB overdrafts and interferences of 75707 were just under the limit. According to Tables B.1 and B.3, overdrafts of DIA1 above 40 MHz are

bigger than overdrafts of 75707A. The bigger overdraft of DIA1 was 2.7 dB and is marked in Figure 42 b).

According to Tables B.1 and B.4, more margins smaller than 5 dB but fewer overdrafts were measured from DIA2 than from 75707A. As can be seen from Figure B. 4 c), overdrafts were measured at same frequency range than were from 75707A in Figure B.1 c). As can be seen from Figure 42 c), the highest overdraft was 1.67 dB at frequency around 50 MHz.

Surprisingly, on the wooden board DIA3 was a bit better than 75707A as can be seen from Figure 42 a) and c). According to Table B.5 and Figure B.5 c), only two overdrafts were measured and those were smaller than overdrafts of 75707A listed in Table B.1 and shown in Figure B.1 c). Figure 42 d) shows that also on the wooden board interferences of buck are increased and the bigger overdraft, 0.08 dB, was measured at frequency 60 MHz.

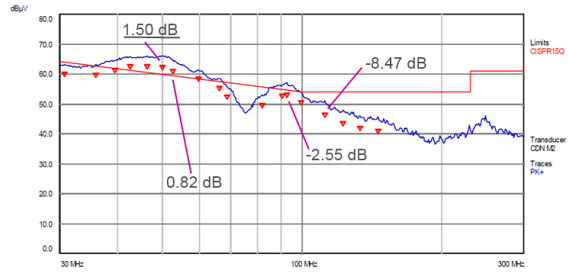
Figure B.6 c) shows that five overdrafts between frequencies 40 MHz and 60 MHz were measured from DIA4. According to Tables B.1 and B.6, overdrafts were overall bigger than overdrafts of 75707A. The highest overdraft was 1.84 dB as marked in Figure 42 e).

The highest overdraft, 5.25 dB, was measured from DIB5 at frequency around 60 MHz as shown in Figure 42 f). From Figure B.7 c) and Table B.7 can be seen that measured interferences were higher up to 90 MHz than were measured from any other PCB.

As shown in Figures 42 a) and g), interferences were over the 5 dB margin at same frequency range as there were overdrafts and small margins in 75707A. According to Table B.9 and Figure B.9 c), DIB6 had only two slight overdrafts. The bigger one, 0.62 dB, was measured at 60 MHz frequency as it is marked in Figure 42 g).

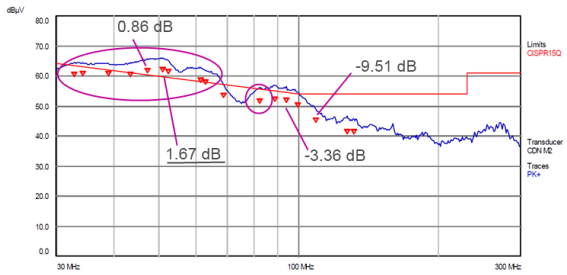
At frequencies between 40 MHz to 65 MHz interferences measured from DIB7 were at limit as shown in Figure 42 h) and in Figure B.10 c). According to Table B.10, only one slight 0.02 dB overdraft was measured, which was a better result corresponding to four overdrafts of 75707A in Table B.1. The overdraft was measured at frequency just under 60 MHz as shown in Figure 42 h).

As shown in Figures 42 a) and i), the biggest difference between DIB8 and 75707A was that the highest overdraft, 1.33 dB, was measured at frequency around 60 MHz on DIB8 when the biggest overdraft of 75707A was measured at 10 MHz lower frequency. As listed in tables B.1 and B.11, the overdrafts of DIB8 were overall slightly smaller than overdrafts of 75707A. This can be seen also from Figures B.1 c) and B.11 c).

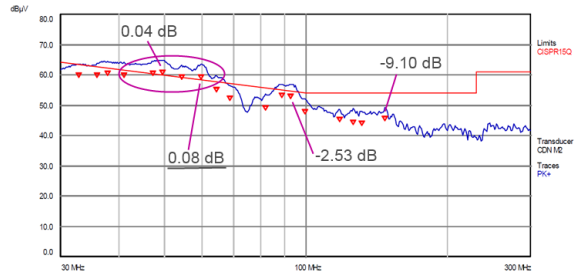


a) 75707A

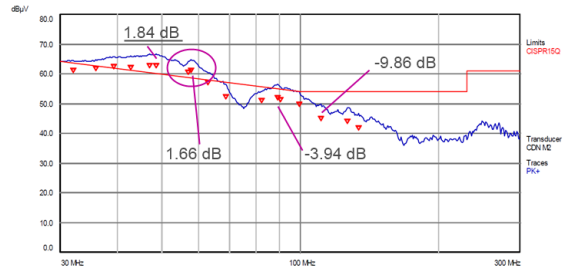
b) DIA1



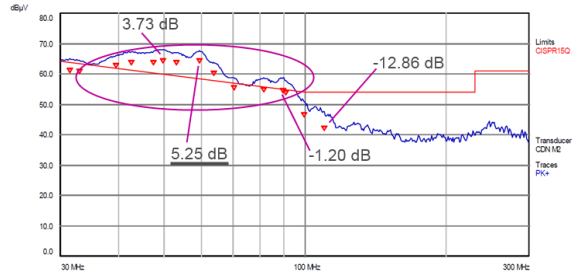
c) DIA2



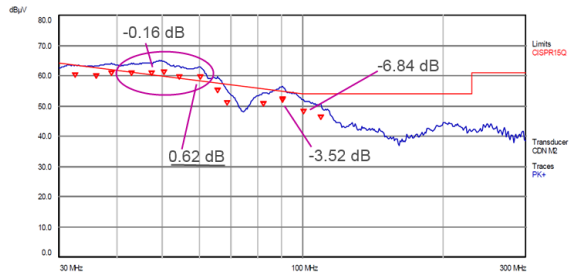
d) DIA3



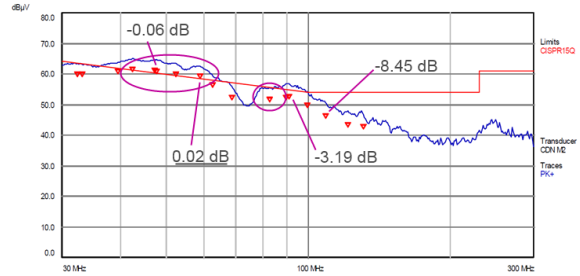
e) DIA4



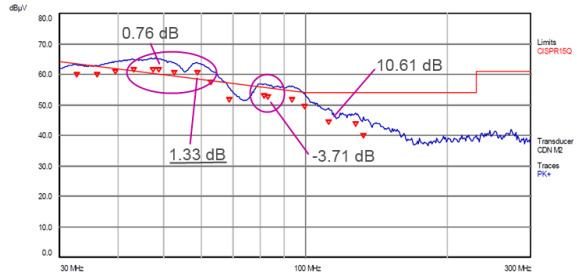
f) DIB5



g) DIB6



h) DIB7



i) DIB8

Figure* 42.Radiated emission pre-measurement results on the wooden board without ground.*

All tested PCBs had overdrafts and margins smaller than 5 dB without ground on the wooden board. Highest overdrafts, quantities of both overdrafts and margins smaller than 5 dB are listed in Table 9 according to tables in Appendix B.

Table 9. *Comparison of results on the wooden board without ground.*

PCB	Final Measurement [pcs.]	Highest overdraft [dB]	Frequency [MHz]	Overdrafts [pcs.]	Margins < 5dB [pcs.]
75707A	18	1.50	49.96	4	8
DIA1	18	2.70	58.64	6	7
DIA2	17	1.67	50.88	3	11
DIA3	18	0.08	59.72	2	9
DIA4	17	1.84	48.64	5	6
DIB5	15	5.25	63.96	7	6
DIB6	15	0.62	60.4	2	9
DIB7	17	0.02	58.8	1	11
DIB8	17	1.33	59.04	4	8

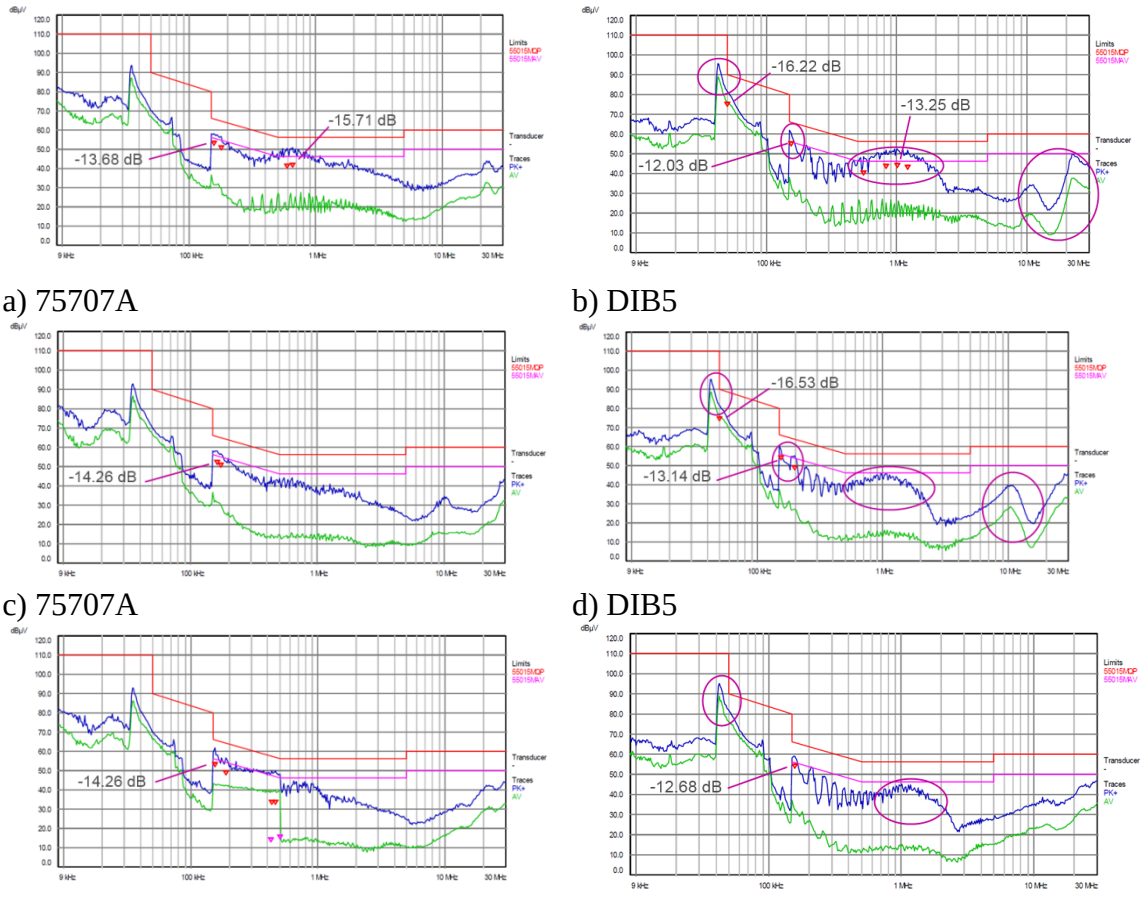
Four overdrafts were measured from the reference PCB and the highest was 4.5 dB. DIB7 had the best result with only one very slight 0.02 dB overdraft. Two second best results were got from DIA3 and DIB6. Both had two overdrafts. Bigger overdraft measured from DIA3 was only 0.08 dB and from DIB6 0.62 dB. Results of DIA2 and DIB8 were almost similar to 75707A. DIA2 had three overdrafts and highest was 1.67 dB. The highest overdraft of the four overdrafts of DIB8 was 1.33 dB. DIA1 and DIB5 were clearly two worst PCBs on the wooden board. Six overdrafts were measured from DIA1 and the highest overdraft was 2.7 dB. The highest overdraft of DIB5 was as much as 5.25 dB and a total of seven overdrafts were measured.

5.2.4 Conducted emission results

Conducted emission was measured from reference board 75707A and DIB5, which has a different RFI-filter. All pre-measurement results of 75707A and DIB5 are presented in Figure 43. At the left side in Figures 43 a), c) and e) are results of 75707A and right side in Figures b), d) and f) results of DIB5. Some margins from final measurements are marked in Figure 43. Pre-measurement results of 75707A can be found in Figure B.2 a) - c) in bigger pictures and final measurements in Table B.2. For DIB5 pre-measurements can be found from Figure B.8 and Table B.8.

First peaks originate from the minimum frequency of the pre-converter. First peaks were slightly bigger and at about 500 Hz higher frequency in DIB5 than in 75707A with all test setups. Narrowest margins were measured at second peak frequencies, which are the maximums of the pre-converter. As shown in Figure 43, measured margins from DIB5 were about 1 dB smaller than from 75707 in all measurements. From Figures 43

b), d) and f) can be also seen higher interferences around 1 MHz in all measurements of DIB5. As can be seen in Figures a), c) and e) corresponding higher interferences, but not as remarkable, are around 600 kHZ.



a) 75707A b) DIB5

c) 75707A d) DIB5

e) 75707A f) DIB5

Figure 43.*Conducted emission pre-measurements results. a) 75707A with ground, b) DIB5 with ground, c) 75707A on the metal plate without ground, d) DIB5 on the metal plate without ground, e) 75707 on the wooden board without ground and f) DIB5 on the wooden board without ground.*

According to Table B.2, final measurements were taken from 75707A also around 600 kHz and from DIB5 around 1 MHz with ground. As shown in Figures 43 a) and b), the smallest measured margin around 1 MHz of DIB5 was about 2.5 dB smaller than measured from 75707A around 600 kHz. At the end of frequency range higher interferences were measured from DIB5 as shown in Figure B.8. With ground, those peaks were after 10 MHz and 20 MHz. Without ground the point was about 10 MHz.

From Figure B.2 c), it can be seen that interferences of 75707 are quite constant between frequencies 200 kHz and 500 kHz on the wooden board, especially in average measurement. This was a result from an error in test equipment, which occurs when bandwidth changes. Final measurement in Table B.2 shows that margins were over 24 dB, which proves that there must be an error in pre-measurement.

6 CONCLUSION

Features of PCB layout effecting on EMC are examined through literature review and experimentally in this thesis. Chapter 2 introduces basic principles behind EMI. EMI problem can occur if an interference source, a receptor and coupling path are present. Time-varying current produces electronic and magnetic fields which can cause interferences. EMI is caused by many variables and one reason is non-ideal behavior of passive components. Coupling methods can be divided on conductive, capacitive, inductive and radiated coupling.

Common PCB design principles considering of EMI are presented in Chapter 3. The main principles pertains segmentation, grounding, tracking and components placement. All good principles can be rarely implemented and compromises needs to be done in PCB design. Good PCB design is very cost-effective way take into account EMC considerations and counter wise, poor layout may produce big problems.

In the beginning of Chapter 4 the examined LED driver and the complied standards are introduced. Also learned matters from previous projects and design rules for manufacturability are represented. Eight PCBs for experiments were designed and produced and they are presented at the end of chapter. Test PCBs were named DIA1-DIA4 and DIB5-DIB8. In each PCB, only one detail was changed, if it was possible. The target is to investigate effects of features, that can be implemented in this kind products, and solve, which features are the most important to be optimized.

Measurements and test results are presented in Chapter 5. Measurements were done at Helvar's RFI chamber according to typical type tests. Radiated emissions were measured from all test PCBs and from the reference PCB. Conducted emissions were measured only from the reference PCB and from one test PCB. Both emissions were measured with ground on the metal plate, without ground on the metal plate and on the wooden board. Measurement results are presented and discussed in the order of test setup. Radiated emission results are introduced first at the following order; with ground, without ground on the metal plate and without ground on the wooden board. Conducted emissions are presented after radiated emissions.

Considering measurement results in all test setups, DIA1 was the worst. Hence the conclusion is that width of ground trace has the most significant effect on interferences from examined features. This was quite unexpected. The bigger main loop in DIA2 had not even close as much effect on interferences. This might be explained with converters loop sizes. Because chokes and capacitors in converter circuits are big and legs are quite far from each other, the current loop is big and can't be made smaller with used components. Second reason might be that PCBs in linear shaped products are relatively

narrow. This feature would be interesting to examine with compact products, in which PCBs are shorter but wider. In conclusion, the main ground should be kept near to the high current trace, but more important is to make the ground as wide as possible.

On the metal plate, differences between radiated emissions of DIB5 and 75707A were quite negligible, but on the wooden board DIB5 was much worse. In DIB5 effect on conducted emissions wasn't significant and margins were so big with both DIB5 and 75707A, that results were not interesting. Hence more traditional RFI-filter without the extra capacitor would be more recommendable in this kind of products.

Results from DIB8 showed clearly, that the supply traces should be routed as straight as possible to first X-capacitor. According to results of DIA4, it is more preferable to ground the current measurement resistors to side of electrolytic capacitor than to second X-capacitor. Results from DIB6 and DIB7 were quite negligible, but also confusing. Both were worse on the metal plate, but better on the wooden board than reference PCB. As well the conclusion of DIA3 wasn't clear. At the buck frequency interferences were higher than is in 75707 in all test conditions, but the biggest differences between measurement results did not seem to be related to functionality of the buck. Maybe PCB was modified too much and some other features were more significant.

The results in this thesis were interesting and can be used in practice to improve PCB designs. Also design rules for manufacturability were collected and harmonized, which was the secondary goal of this thesis. The accuracy of measurement results in this thesis was evaluated as sufficient for this kind of PCB comparison. Reproducibility of the results was improved by for example taping down wires, since the placement of wires in test setup can affect the test results, and making same measurement for all PCBs in sequentially in the same measurement session. The measurement results could have been more accurate and reliable, if measurements would have been done in a better RFI-chamber and for example with field-strength-method. Improving the RFI-chamber should be discussed and although the CDN-method is according to standard, the possibility of field-strength-method should not be forgotten.

After the PCBs for this thesis were designed, order and components were placed, a RFI-problem with traces of pumped supply voltage was noticed. It would be interesting and beneficial to investigate also supply voltage pumping for IC and operational amplifier in the viewpoint of EMC. Another object for this kind of research would be SELV compact products, which have different circuit designs and very different PCBs than examined in this thesis.

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A. APPENDIX

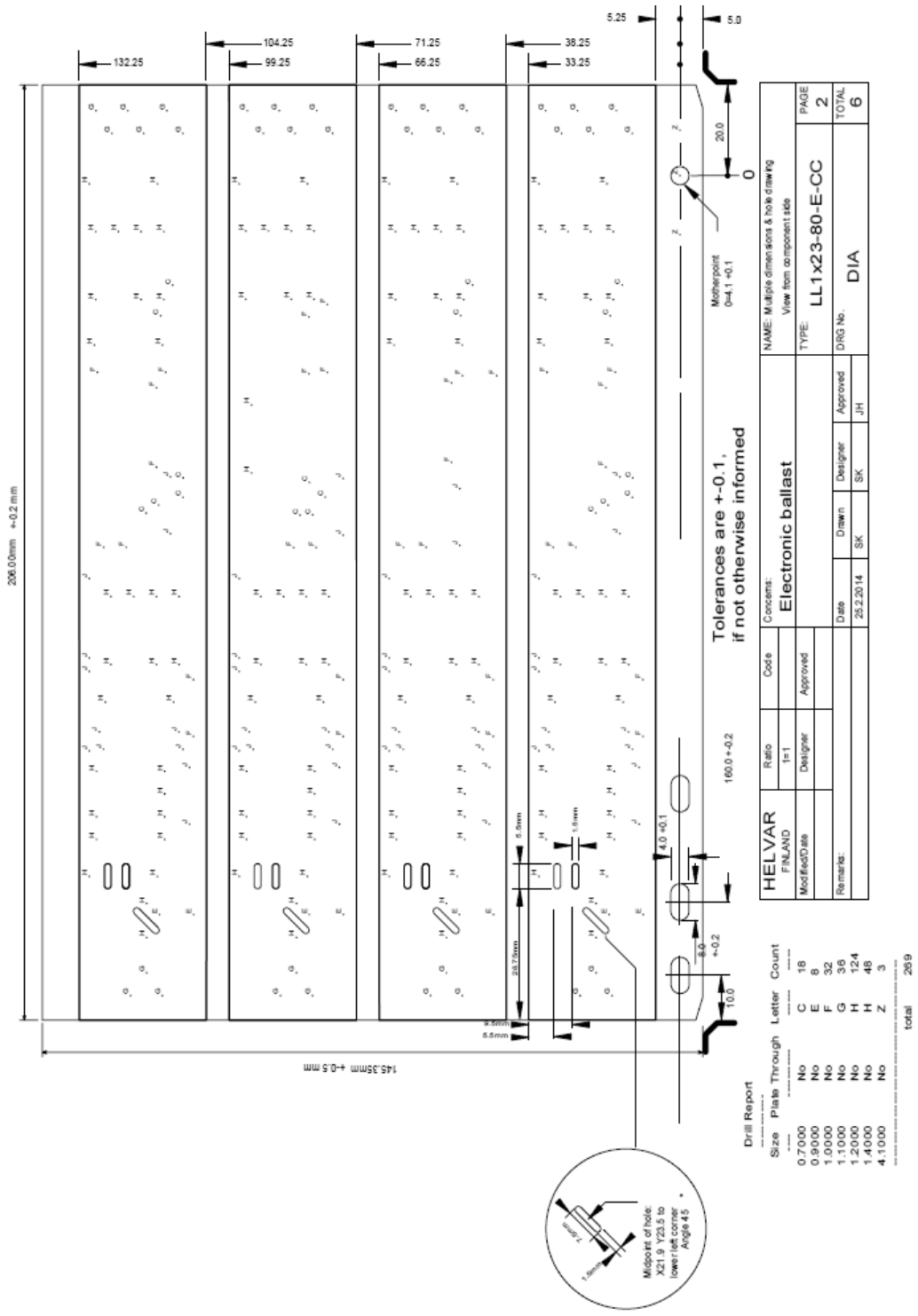


Figure A. 1. *Drill drawing DIA*

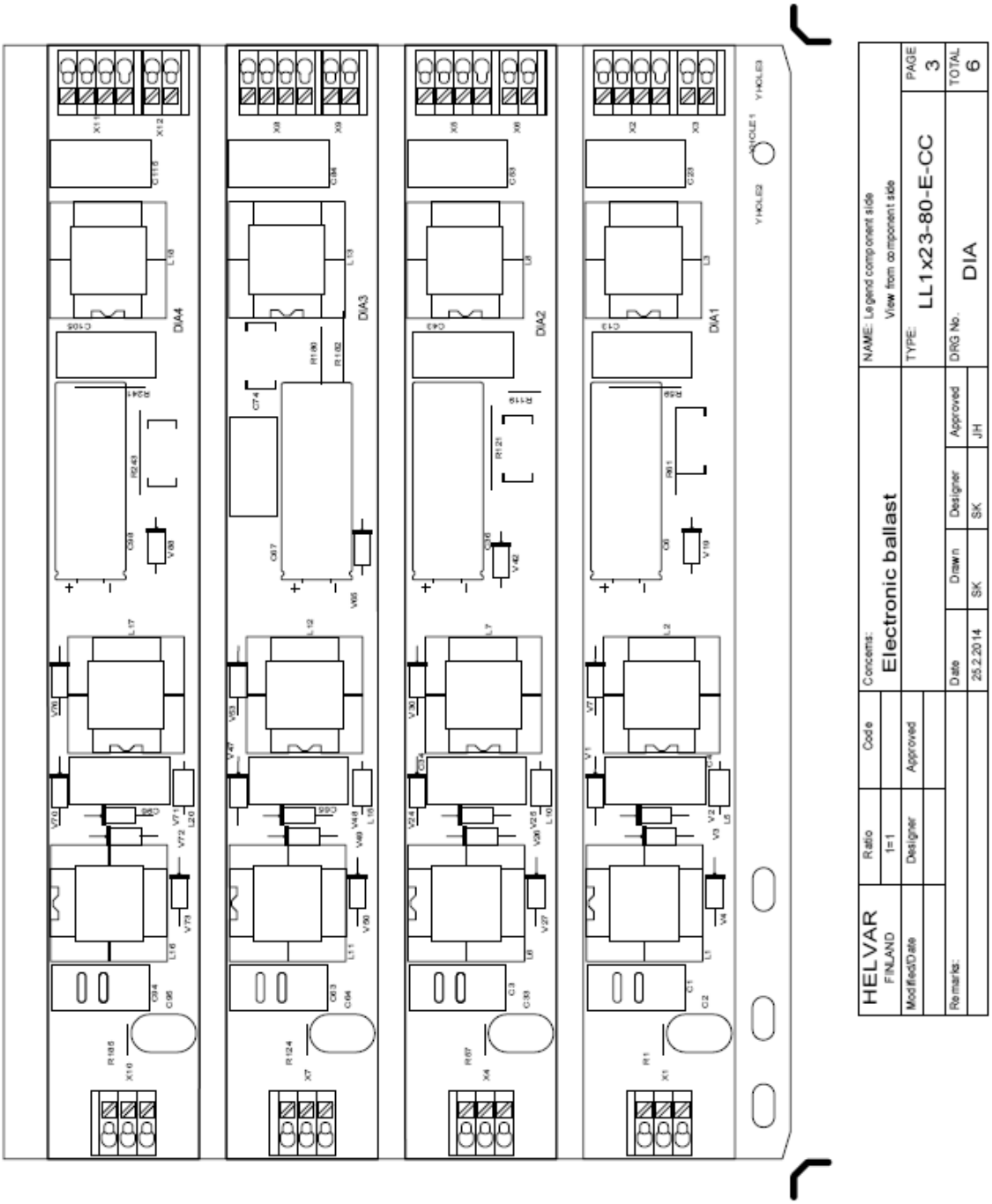


Figure *A. 2.* *Top silk DIA.*

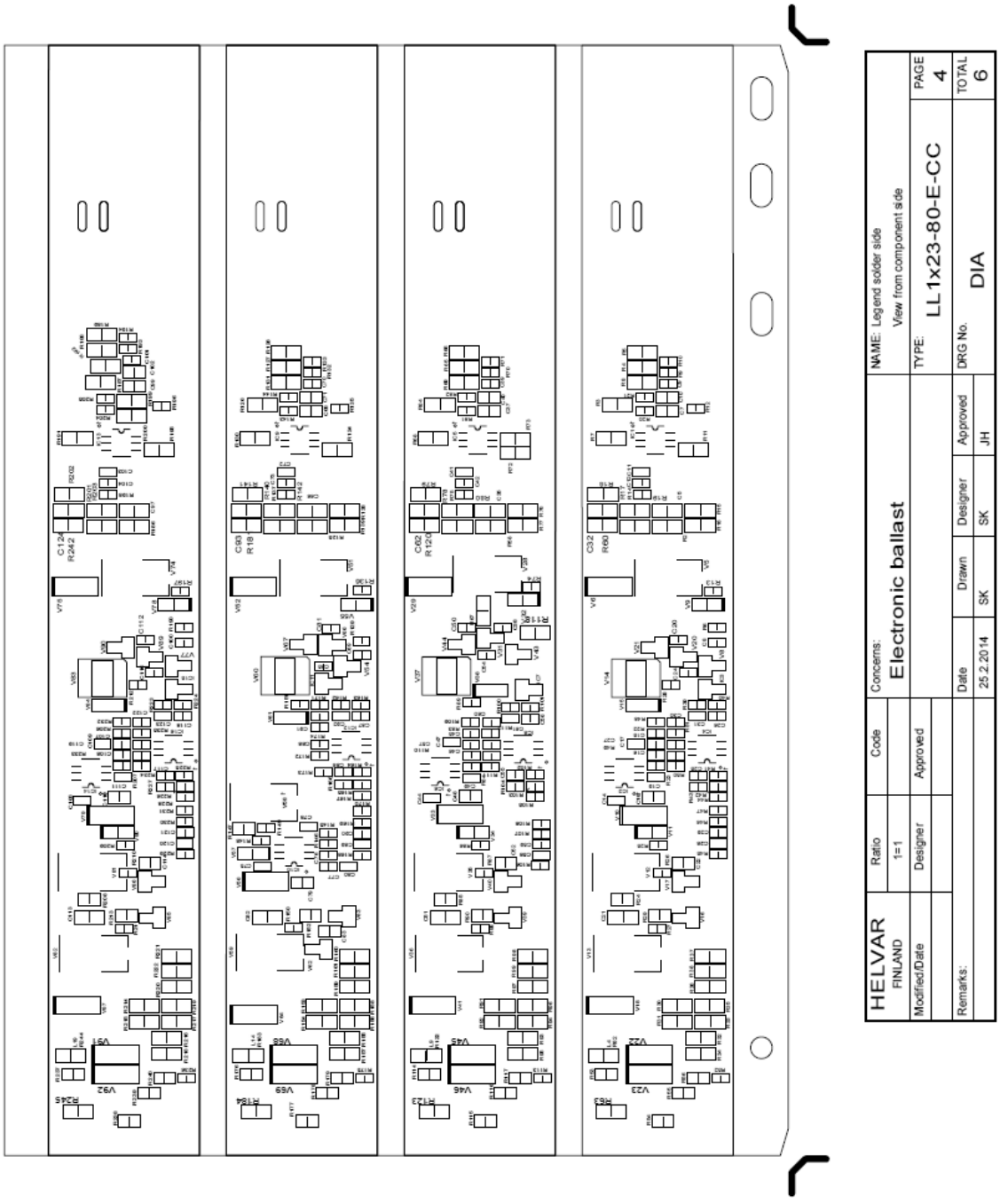


Figure A. 3. *Bottom silk DIA.*

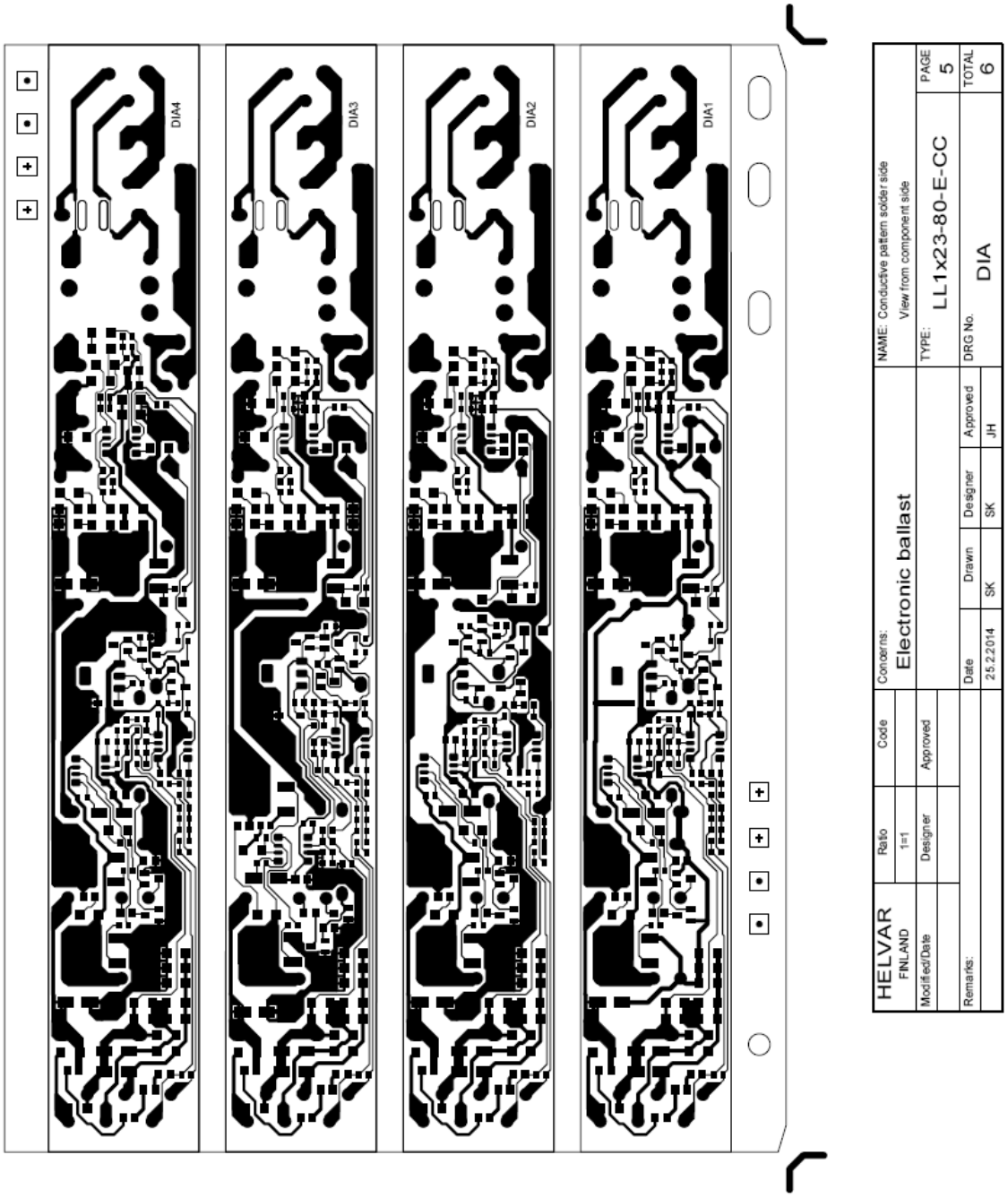


Figure A. 4. *Bottom copper DIA.*

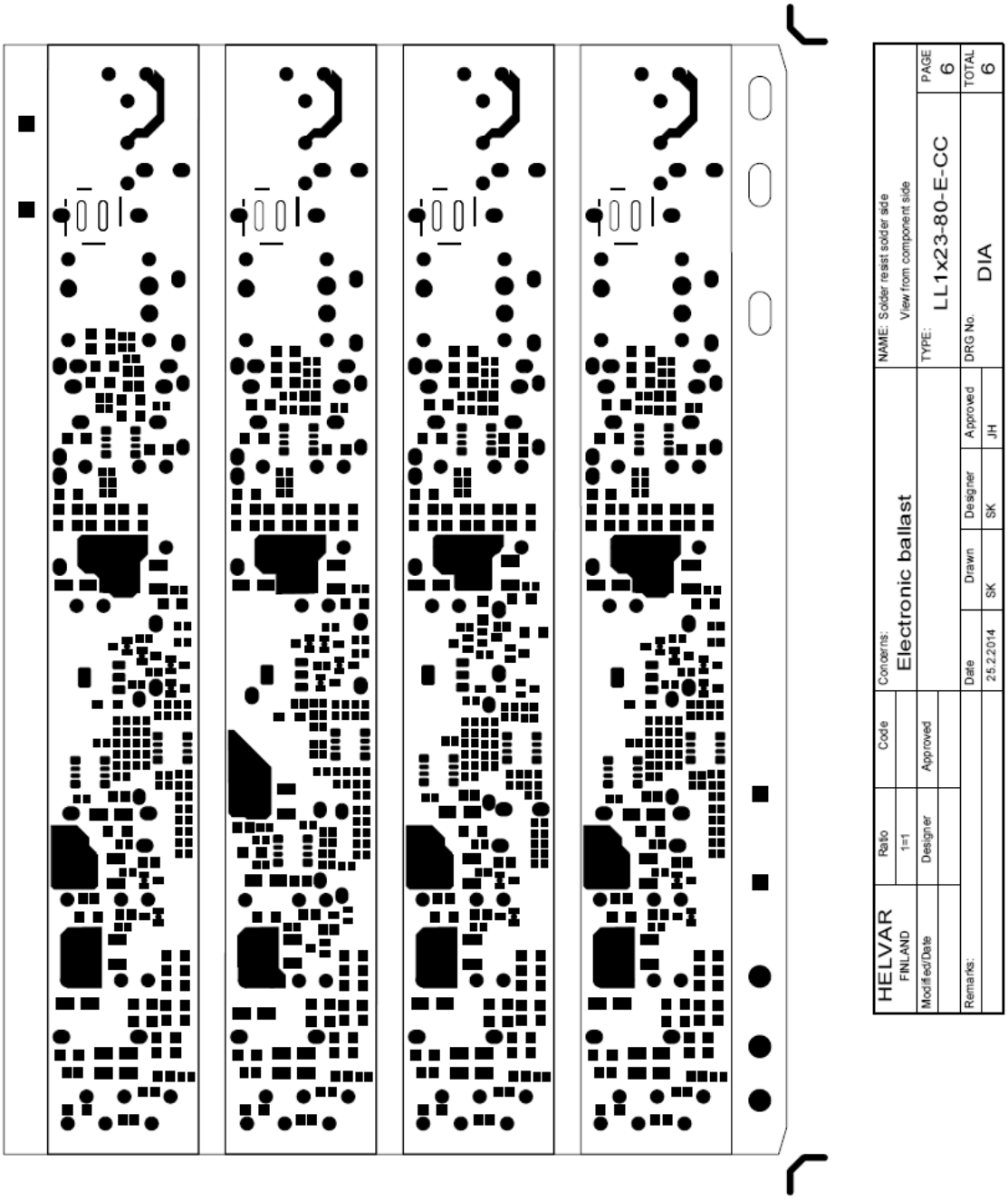


Figure A. 5. *Bottom solder resist DIA.*

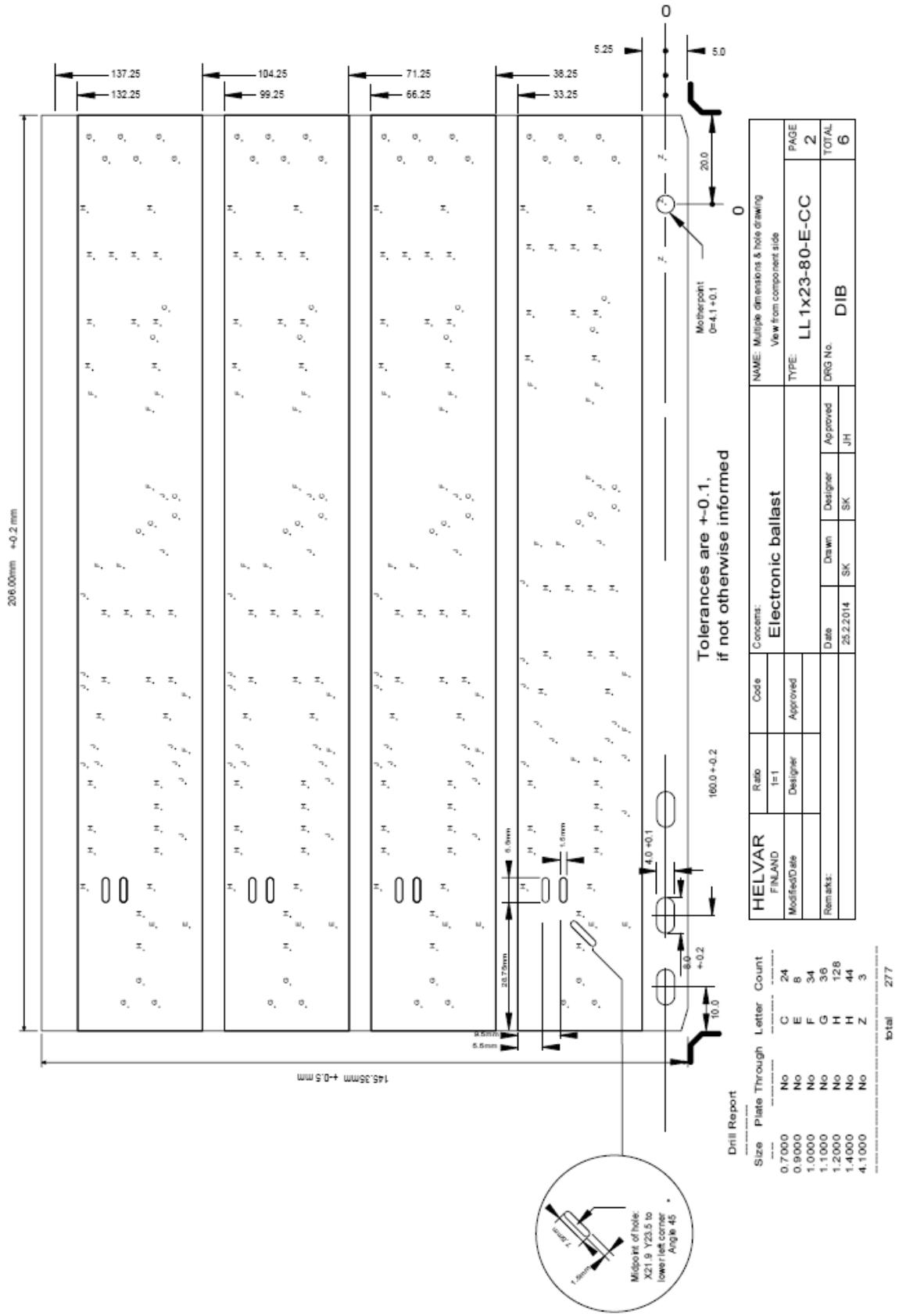


Figure A. 6. *Drill drawing DIB.*

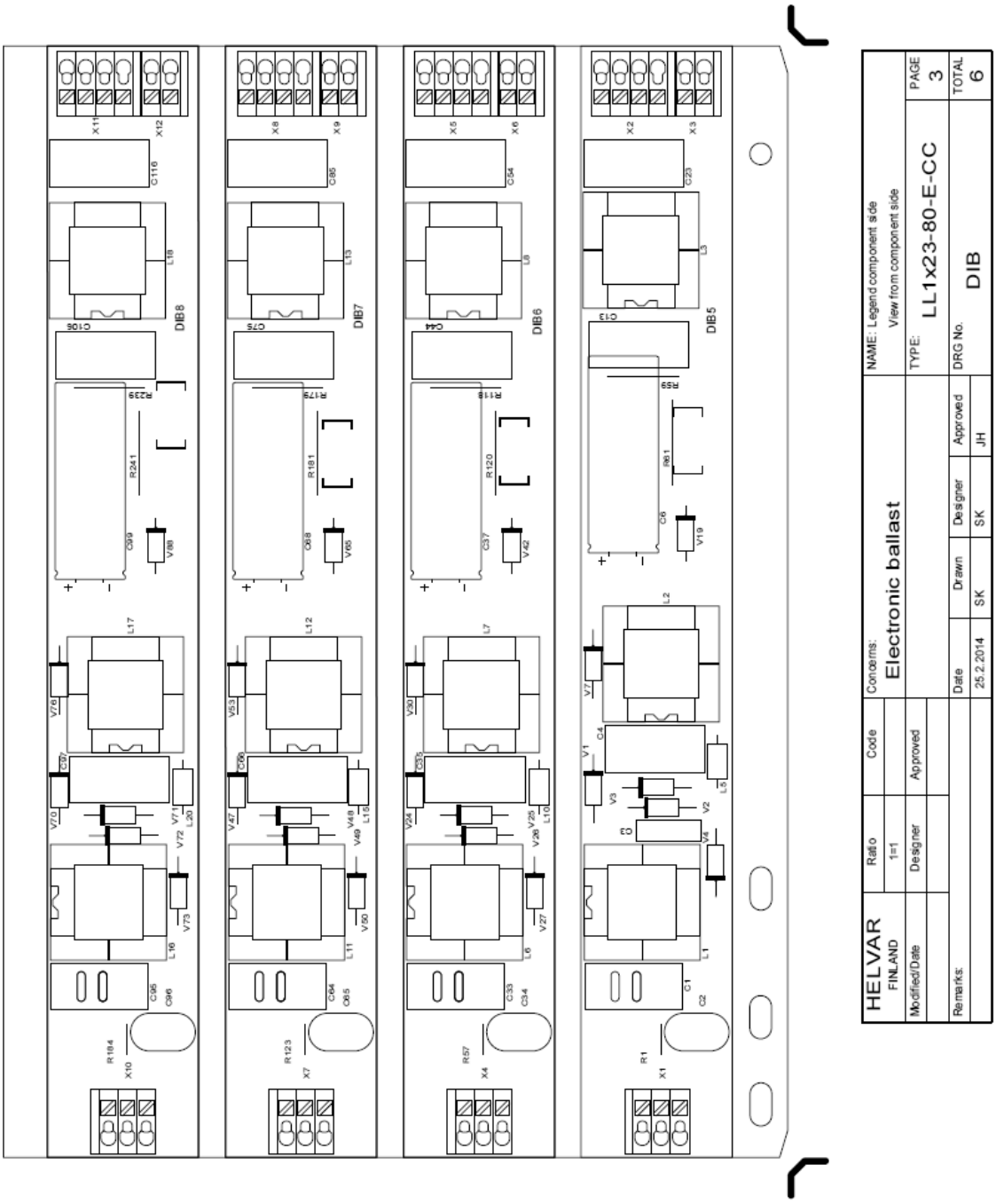


Figure A. 7. *Top silk DIB.*

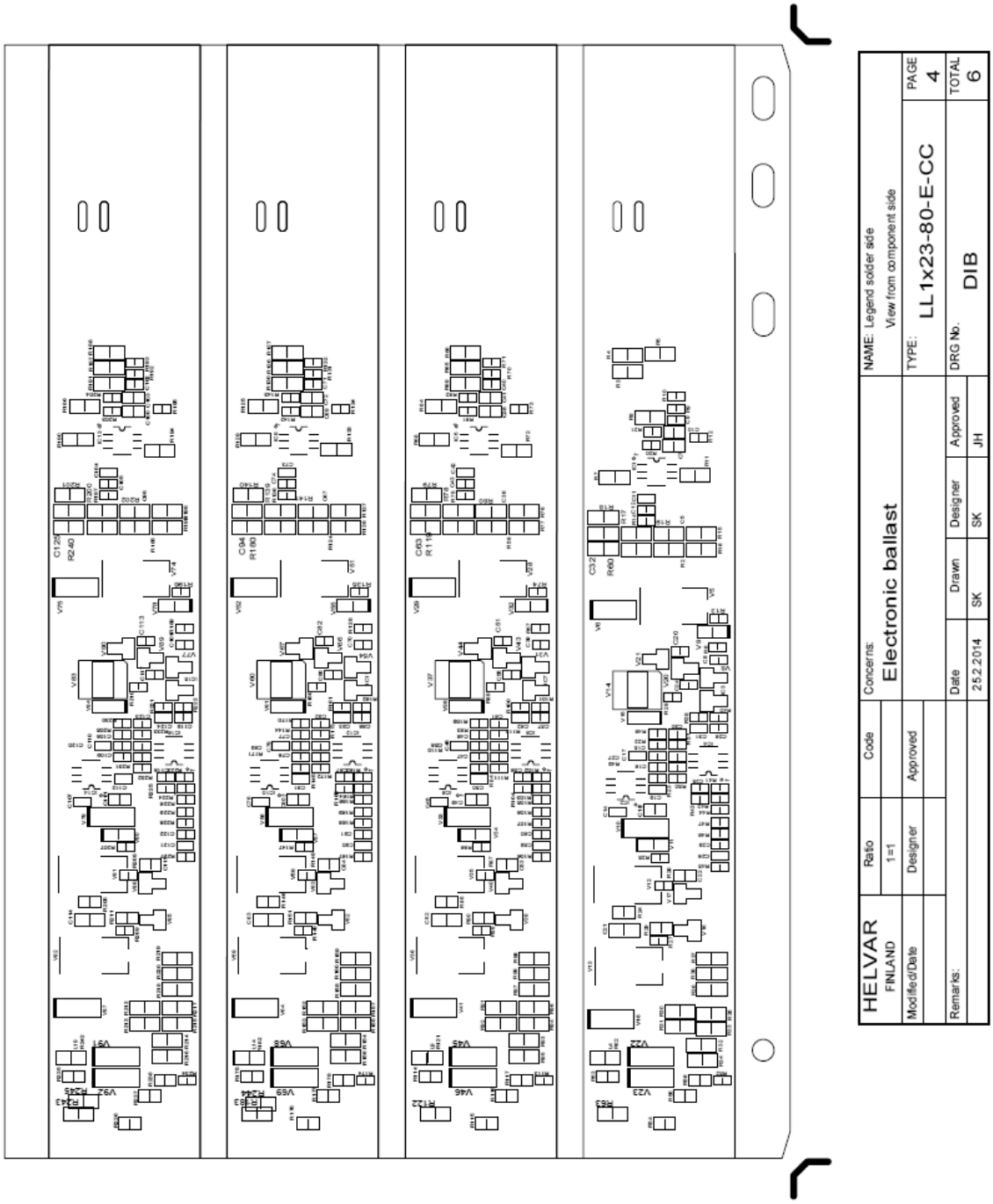


Figure A. 8. *Bottom silk DIB.*

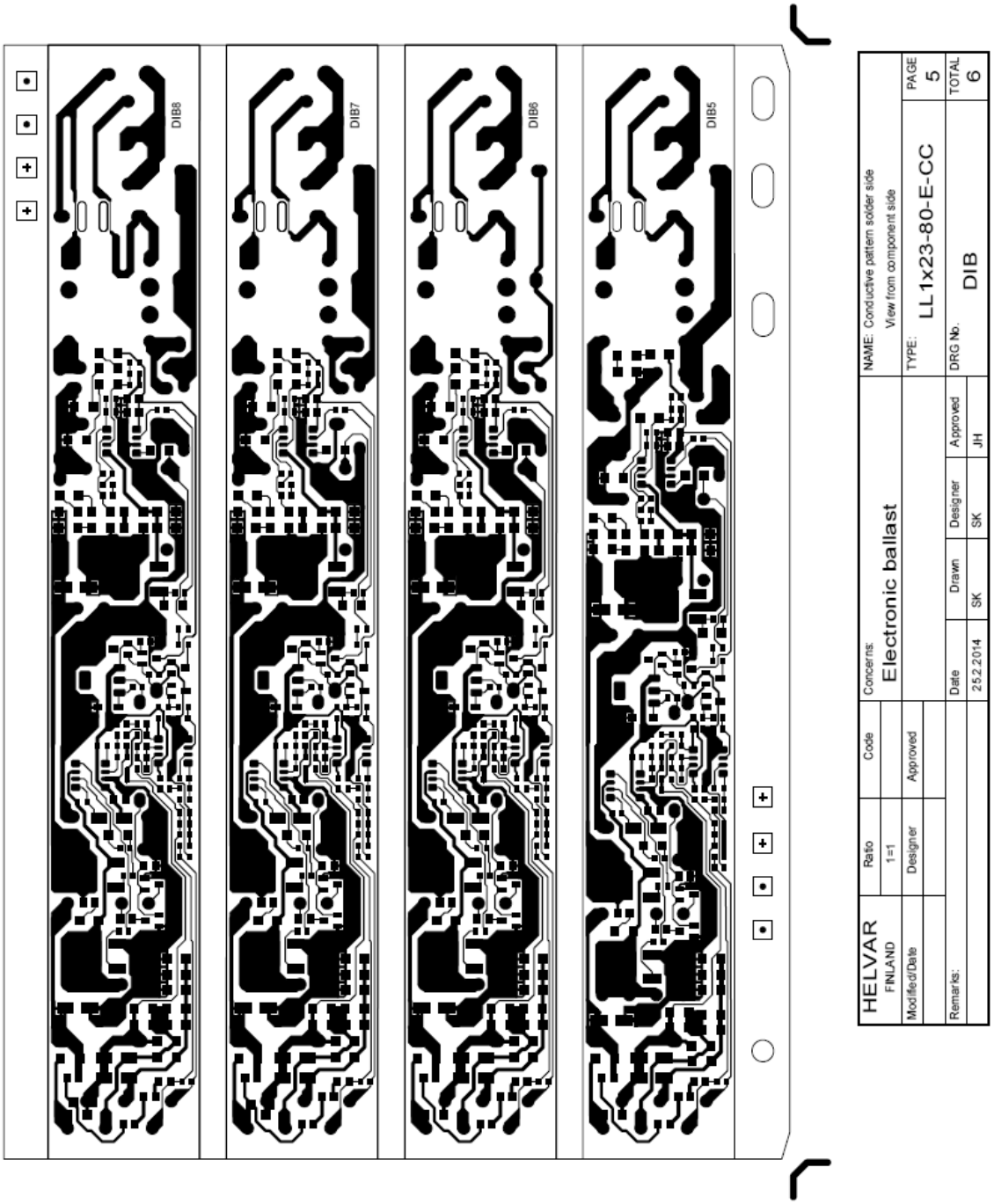


Figure A. 9. *Bottom copper DIB.*

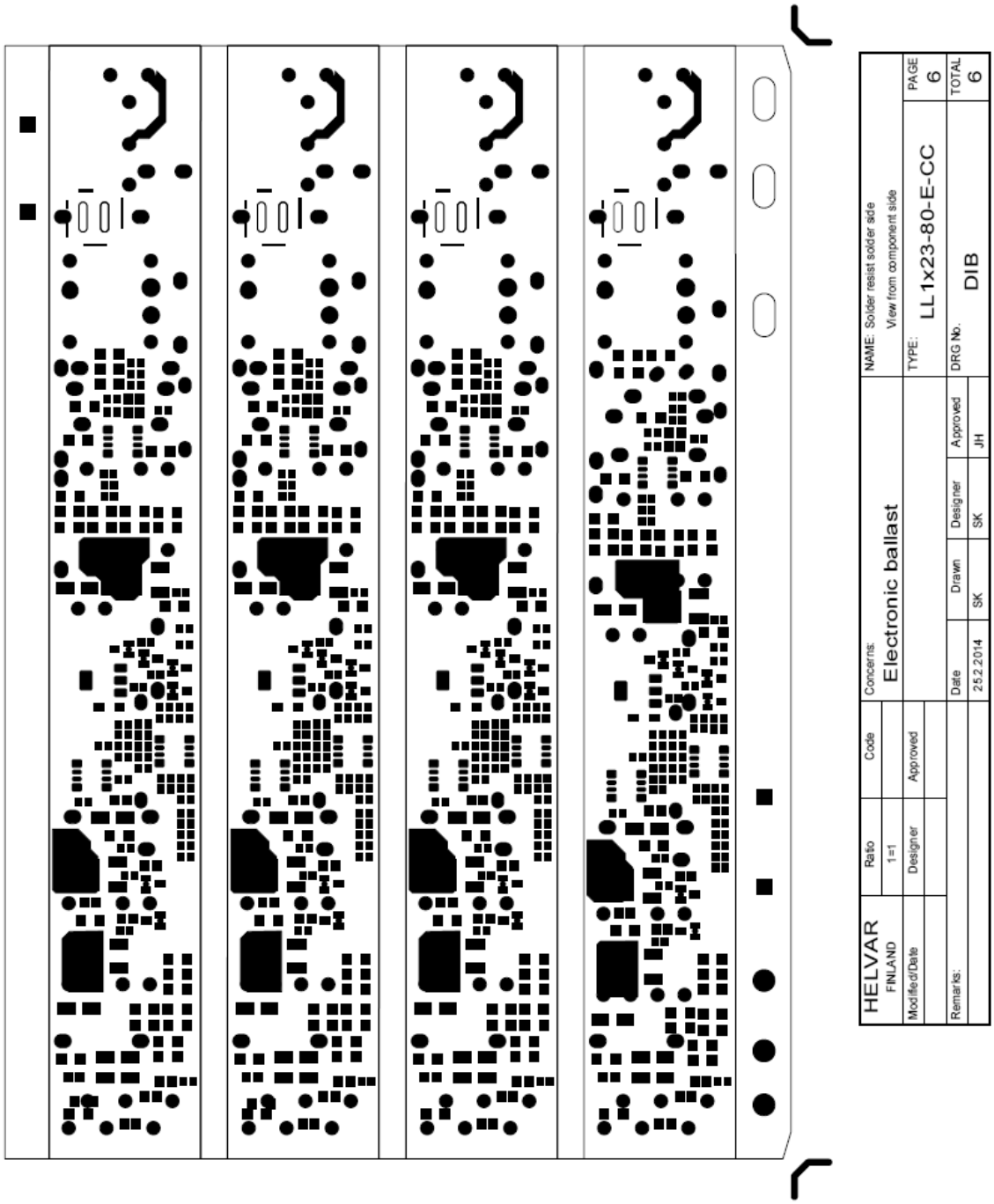
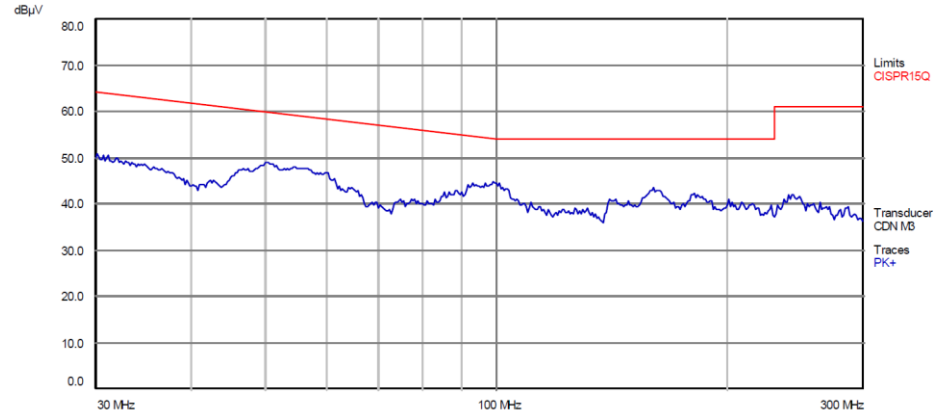


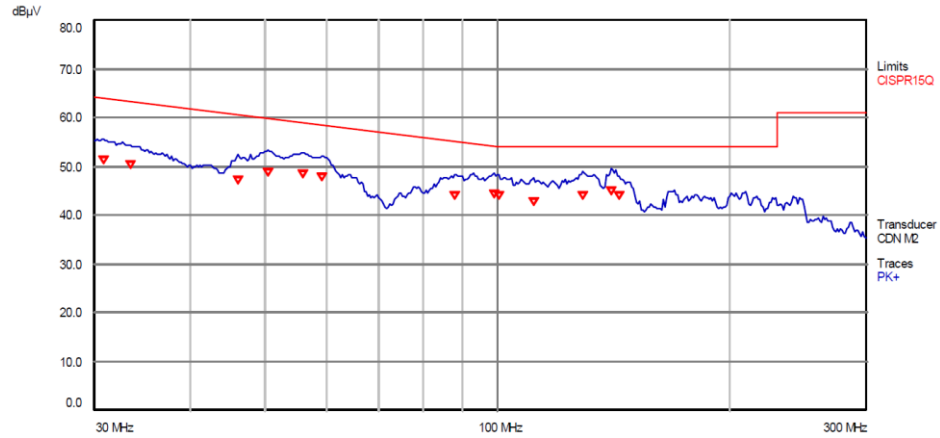
Figure A. 10. *Bottom solder resist DIB.*

B. APPENDIX

a)



b)



c)

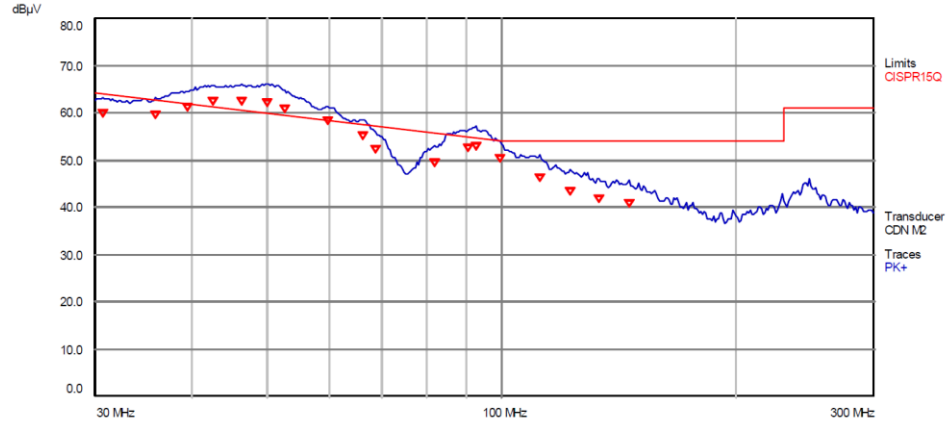
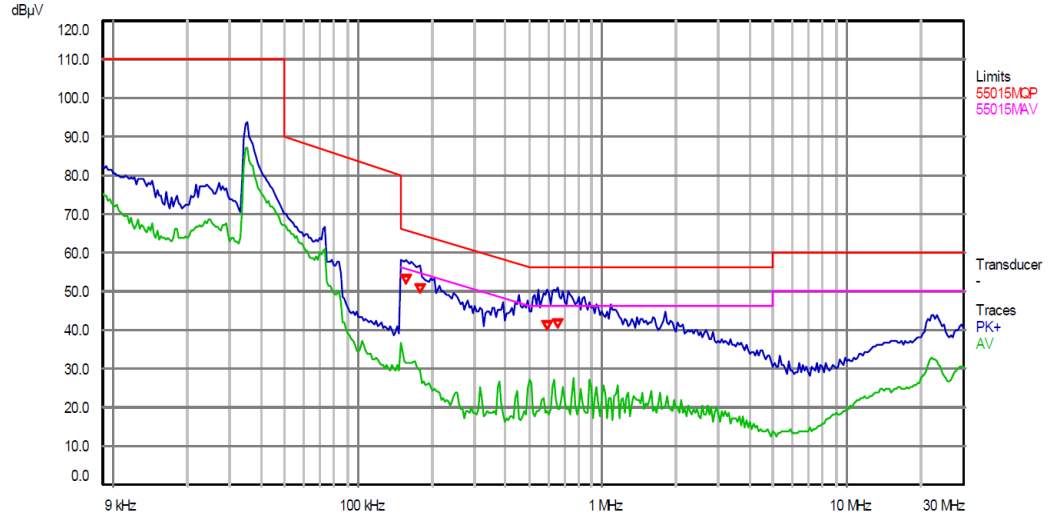


Figure B. 1. *Radiated emission pre-measurement results of 75707A, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

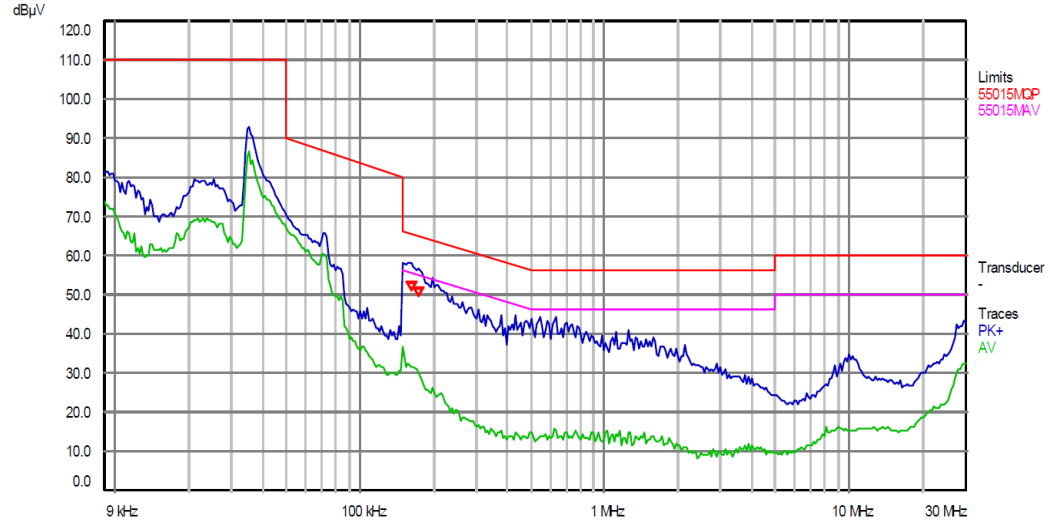
Table B.1. *Radiated emission final measurement results of 75707A.*

Metal plate					
1	QP	30.88	50.47	63.76	-13.29
1	QP	33.44	49.54	63.10	-13.56
1	QP	46.04	46.50	60.44	-13.94
1	QP	50.52	48.03	59.67	-11.64
1	QP	55.88	47.48	58.83	-11.35
1	QP	59.12	47.03	58.37	-11.34
1	QP	88.04	43.33	55.06	-11.73
1	QP	98.88	43.50	54.09	-10.59
1	QP	100.24	43.20	54.00	-10.80
1	QP	111.36	41.89	54.00	-12.11
1	QP	129.04	43.25	54.00	-10.75
1	QP	140.6	44.01	54.00	-9.99
1	QP	143.88	43.10	54.00	-10.90
Wooden board					
1	QP	30.76	59.02	63.79	-4.77
1	QP	35.88	58.72	62.51	-3.79
1	QP	39.44	60.44	61.73	-1.29
1	QP	42.6	61.47*	61.09	0.38
1	QP	46.28	61.52*	60.40	1.120
1	QP	49.96	61.26*	59.76	1.500
1	QP	52.56	60.16*	59.34	0.82
1	QP	59.88	57.54	58.26	-0.72
1	QP	66.32	54.22	57.41	-3.19
1	QP	68.96	51.36	57.09	-5.73
1	QP	81.96	48.51	55.65	-7.14
1	QP	90.52	51.87	54.83	-2.96
1	QP	92.44	52.10	54.65	-2.55
1	QP	99.36	49.48	54.05	-4.57
1	QP	112.08	45.53	54.00	-8.47
1	QP	122.12	42.59	54.00	-11.41
1	QP	133.36	40.95	54.00	-13.05
1	QP	145.48	40.15	54.00	-13.85

a)



b)



c)

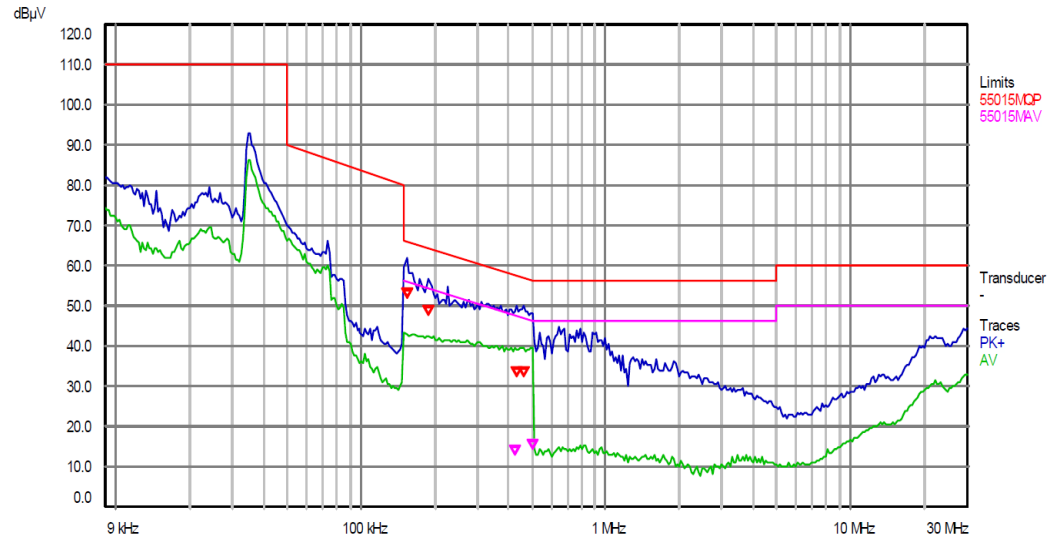
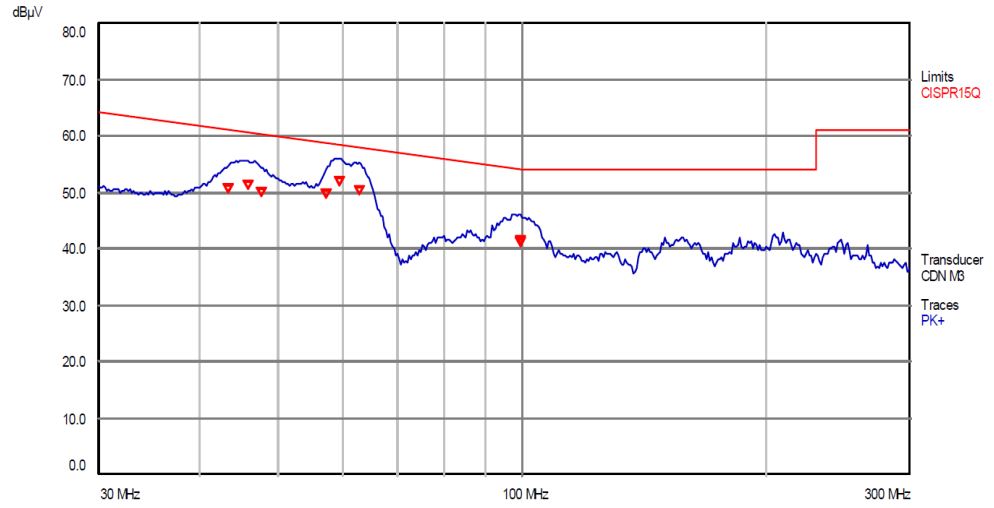


Figure B. 2. *Conducted emission pre-measurement results of 75707A, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

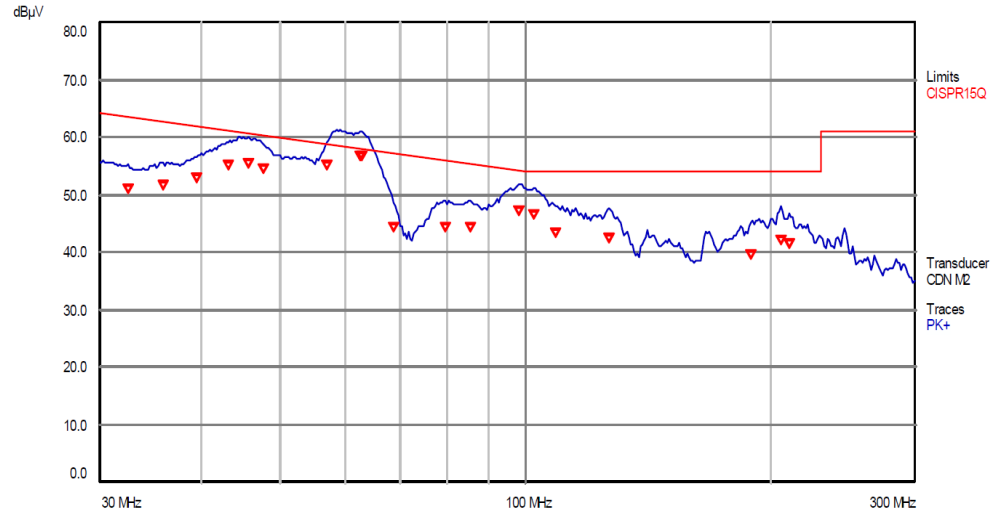
Table B.2. *Conducted emission final measurement results of 75707A.*

With ground					
1	QP	0.158	51.89	65.57	-13.68
1	QP	0.178	49.53	64.58	-15.05
1	QP	0.59	39.92	56.00	-16.08
1	QP	0.658	40.29	56.00	-15.71
Metal plate					
1	QP	0.162	51.10	65.36	-14.26
1	QP	0.174	49.74	64.77	-15.03
Wooden board					
1	QP	0.154	52.11	65.78	-13.67
1	QP	0.19	47.72	64.04	-16.32
2	AV	0.426	12.750	47.33	-34.58
1	QP	0.434	32.29	57.18	-24.89
1	QP	0.462	32.44	56.66	-24.22
2	AV	0.502	14.32	46.00	-31.68

a)



b)



c)

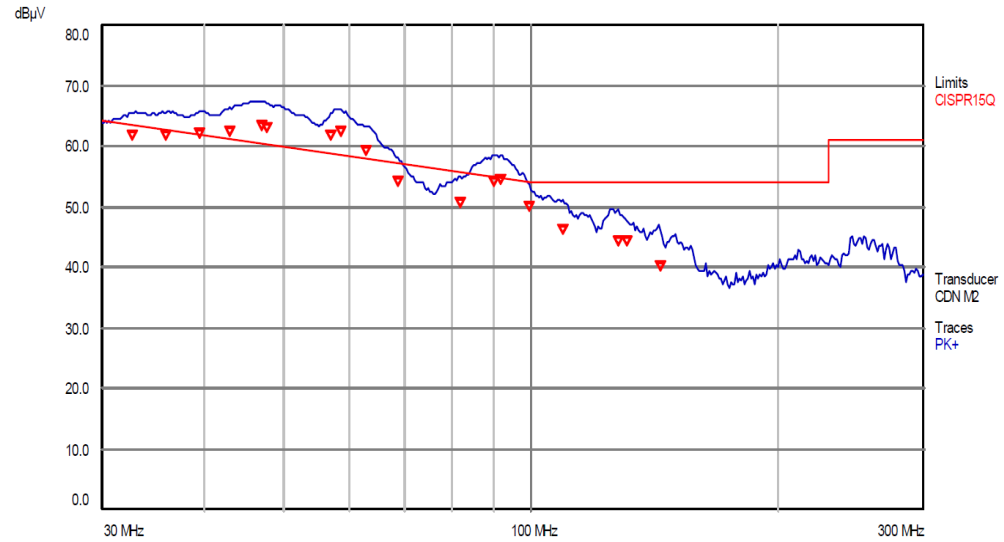
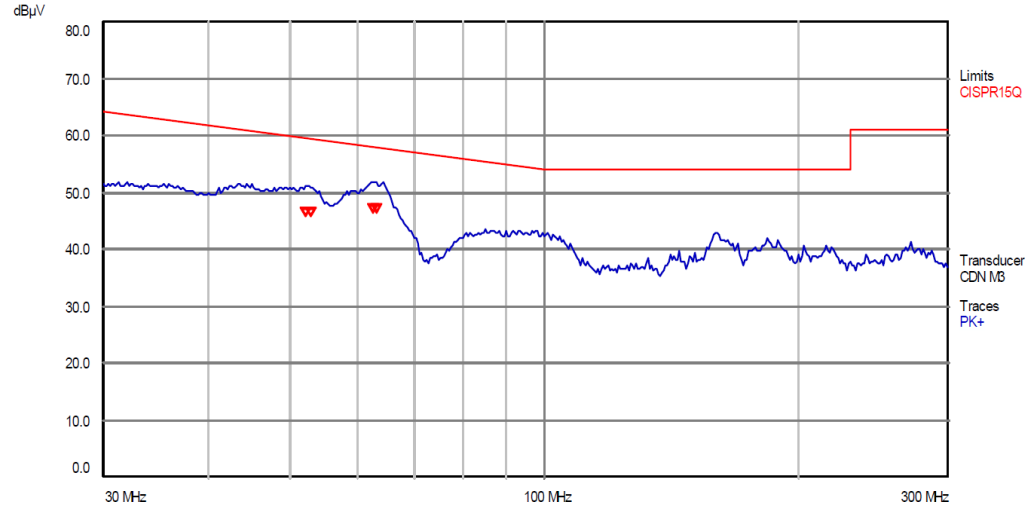


Figure B. 3. *Radiated emission pre-measurement results of DIA1, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

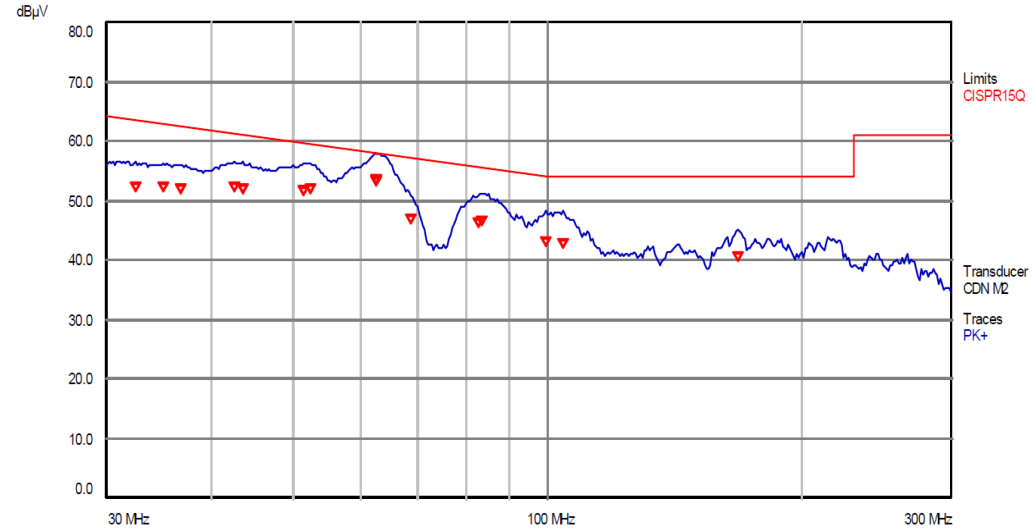
Table B.3. *Radiated emission final measurement results of DIA1.*

With ground											
1	QP	43.32	49.72	60.95	-11.23						
1	QP	45.8	50.46	60.49	-10.03						
1	QP	47.68	49.16	60.15	-10.99						
1	QP	57.16	48.82	58.65	-9.83						
1	QP	59.44	51.01	58.32	-7.31						
1	QP	62.8	49.57	57.86	-8.29						
1	QP	99.24	40.52	54.06	-13.54						
1	QP	99.64	40.44	54.03	-13.59						
Metal plate						Wooden board					
1	QP	32.48	50.26	63.34	-13.08	1	QP	32.68	60.93	63.29	-2.36
1	QP	35.96	50.80	62.49	-11.69	1	QP	35.96	61.08	62.49	-1.41
1	QP	39.52	52.10	61.71	-9.61	1	QP	39.4	61.36	61.74	-0.38
1	QP	43.12	54.24	60.99	-6.75	1	QP	42.88	61.70*	61.03	0.67
1	QP	45.56	54.75	60.53	-5.78	1	QP	46.88	62.45*	60.29	2.160
1	QP	47.64	53.55	60.16	-6.61	1	QP	47.56	62.34*	60.17	2.170
1	QP	57.04	54.39	58.66	-4.27	1	QP	57.12	60.98*	58.65	2.330
1	QP	62.52	55.78	57.90	-2.12	1	QP	58.64	61.50*	58.43	2.700
1	QP	63.0	55.73	57.84	-2.11	1	QP	62.84	58.55*	57.86	0.69
1	QP	68.84	43.58	57.10	-13.52	1	QP	68.8	53.20	57.11	-3.91
1	QP	79.84	43.53	55.87	-12.34	1	QP	81.8	49.79	55.67	-5.88
1	QP	85.44	43.54	55.31	-11.77	1	QP	90.24	53.22	54.85	-1.63
1	QP	98.28	46.25	54.14	-7.89	1	QP	91.68	53.62	54.72	-1.10
1	QP	102.24	45.75	54.00	-8.25	1	QP	99.52	49.27	54.04	-4.77
1	QP	109.0	42.59	54.00	-11.41	1	QP	109.44	45.50	54.00	-8.50
1	QP	126.36	41.72	54.00	-12.28	1	QP	127.56	43.51	54.00	-10.49
1	QP	188.52	38.68	54.00	-15.32	1	QP	130.96	43.43	54.00	-10.57
1	QP	205.36	41.17	54.00	-12.83	1	QP	144.0	39.43	54.00	-14.57
1	QP	210.6	40.76	54.00	-13.24						

a)



b)



c)

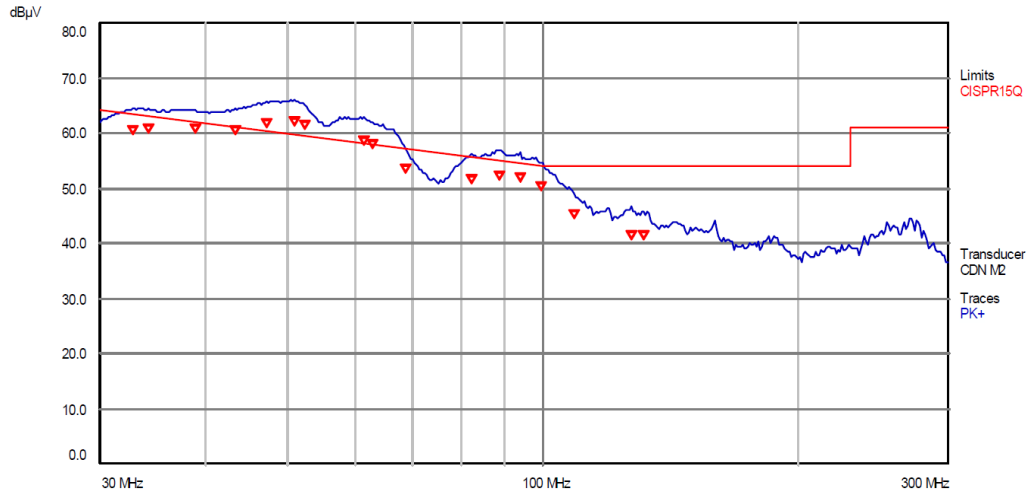


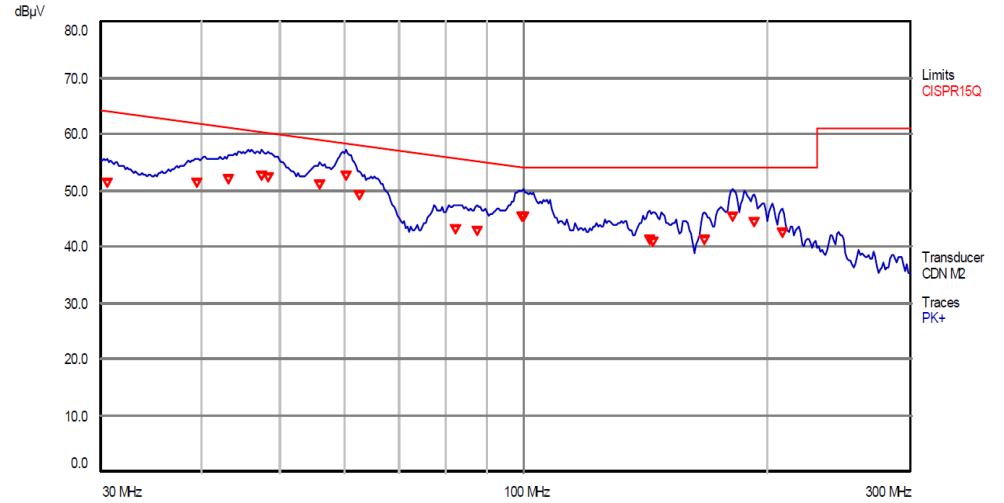
Figure B. 4. *Radiated emission pre-measurement results of DIA2, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

Table B.4. *Radiated emission final measurement results of DIA2.*

With ground					
1	QP	52.08	45.59	59.42	-13.83
1	QP	52.8	45.66	59.30	-13.64
1	QP	62.64	46.48	57.89	-11.41
1	QP	63.2	46.48	57.81	-11.33
Metal plate					
1	QP	32.44	51.37	63.35	-11.98
1	QP	35.08	51.35	62.70	-11.35
1	QP	36.68	51.18	62.33	-11.15
1	QP	42.56	51.28	61.10	-9.82
1	QP	43.48	51.18	60.92	-9.74
1	QP	51.4	50.75	59.53	-8.78
1	QP	52.28	50.99	59.39	-8.40
1	QP	62.56	52.53	57.90	-5.37
1	QP	62.72	52.54	57.87	-5.33
1	QP	68.84	46.00	57.10	-11.10
1	QP	82.6	45.44	55.59	-10.15
1	QP	83.4	45.71	55.51	-9.80
1	QP	99.28	42.14	54.06	-11.92
1	QP	104.2	41.95	54.00	-12.05
1	QP	168.28	39.82	54.00	-14.18
Wooden board					
1	QP	32.84	59.84	63.25	-3.41
1	QP	34.24	59.93	62.90	-2.97
1	QP	38.92	60.15	61.84	-1.69
1	QP	43.32	59.74	60.95	-1.21
1	QP	47.2	61.10*	60.24	0.86
1	QP	50.88	61.28*	59.61	1.670
1	QP	52.4	60.51*	59.37	1.140
1	QP	61.6	57.75	58.02	-0.27
1	QP	62.8	57.11	57.86	-0.75
1	QP	68.76	52.79	57.11	-4.32
1	QP	82.2	50.86	55.63	-4.77
1	QP	88.64	51.55	55.00	-3.45
1	QP	93.8	51.17	54.53	-3.36
1	QP	99.56	49.40	54.04	-4.64
1	QP	109.0	44.49	54.00	-9.51
1	QP	126.88	40.67	54.00	-13.33
1	QP	131.52	40.77	54.00	-13.23

a)

b)



c)

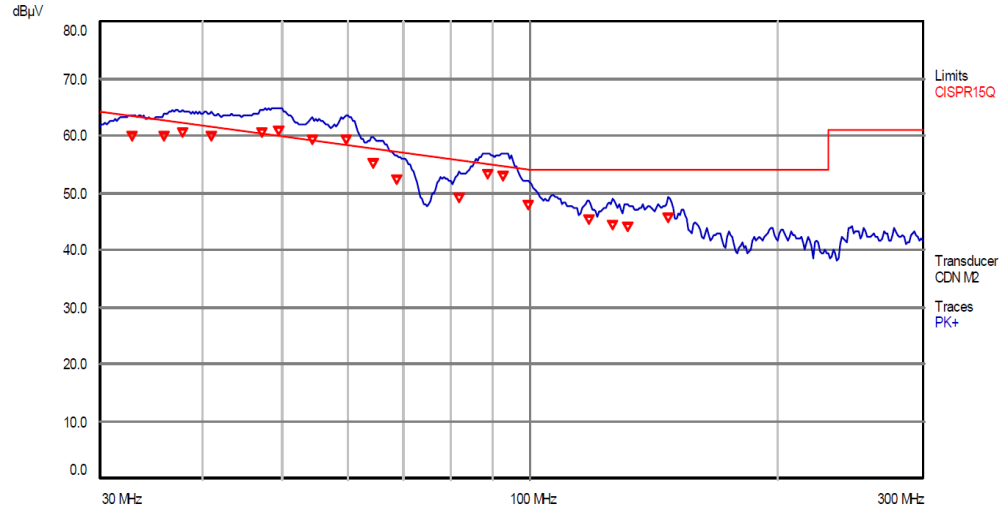
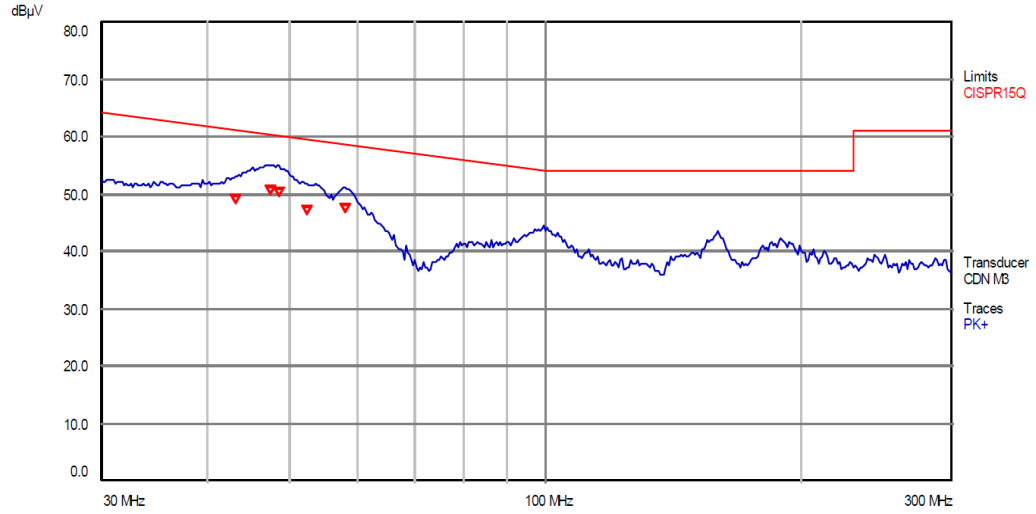


Figure B. 5. *Radiated emission pre-measurement results of DIA3, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

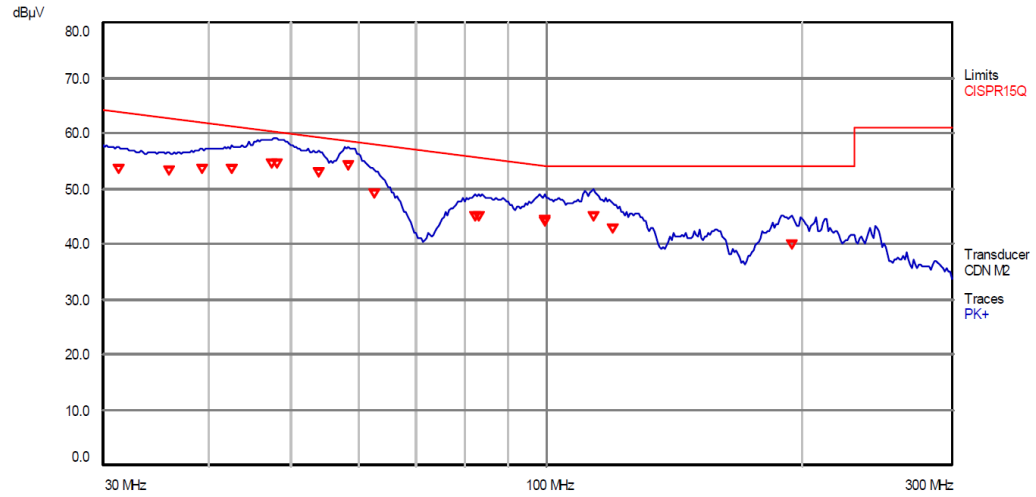
Table B.5. *Radiated emission final measurement results of DIA3.*

With ground											
1	QP	46.16	47.83	60.42	-12.59						
1	QP	48.28	47.43	60.05	-12.62						
1	QP	59.96	45.06	58.25	-13.19						
1	QP	208.52	39.45	54.00	-14.55						
1	QP	186.64	41.70	54.00	-12.30						
1	QP	193.16	40.98	54.00	-13.02						
Metal plate						Wooden board					
1	QP	30.52	50.51	63.86	-13.35	1	QP	32.88	58.94	63.24	-4.30
1	QP	39.48	50.43	61.72	-11.29	1	QP	35.92	59.08	62.50	-3.42
1	QP	43.16	51.17	60.98	-9.81	1	QP	37.88	59.77	62.06	-2.29
1	QP	47.44	51.82	60.19	-8.37	1	QP	40.96	59.02	61.41	-2.39
1	QP	48.32	51.43	60.04	-8.61	1	QP	47.16	59.77	60.24	-0.47
1	QP	55.92	50.30	58.83	-8.53	1	QP	49.48	59.88*	59.84	0.04
1	QP	60.4	51.79	58.19	-6.40	1	QP	54.44	58.28	59.05	-0.77
1	QP	62.76	48.21	57.87	-9.66	1	QP	59.72	58.36	58.28	0.08
1	QP	82.52	42.34	55.60	-13.26	1	QP	64.4	54.39	57.66	-3.27
1	QP	87.44	42.03	55.11	-13.08	1	QP	68.84	51.33	57.10	-5.77
1	QP	99.32	44.45	54.06	-9.61	1	QP	82.08	48.33	55.64	-7.31
1	QP	99.8	44.42	54.02	-9.60	1	QP	88.84	52.41	54.98	-2.57
1	QP	142.8	40.20	54.00	-13.80	1	QP	92.48	52.12	54.65	-2.53
1	QP	144.08	40.15	54.00	-13.85	1	QP	99.56	47.01	54.04	-7.03
1	QP	167.08	40.35	54.00	-13.65	1	QP	117.8	44.42	54.00	-9.58
1	QP	181.24	44.56	54.00	-9.44	1	QP	125.92	43.64	54.00	-10.36
1	QP	192.52	43.38	54.00	-10.62	1	QP	131.68	43.31	54.00	-10.69
1	QP	208.44	41.45	54.00	-12.55	1	QP	147.4	44.90	54.00	-9.10

a)



b)



c)

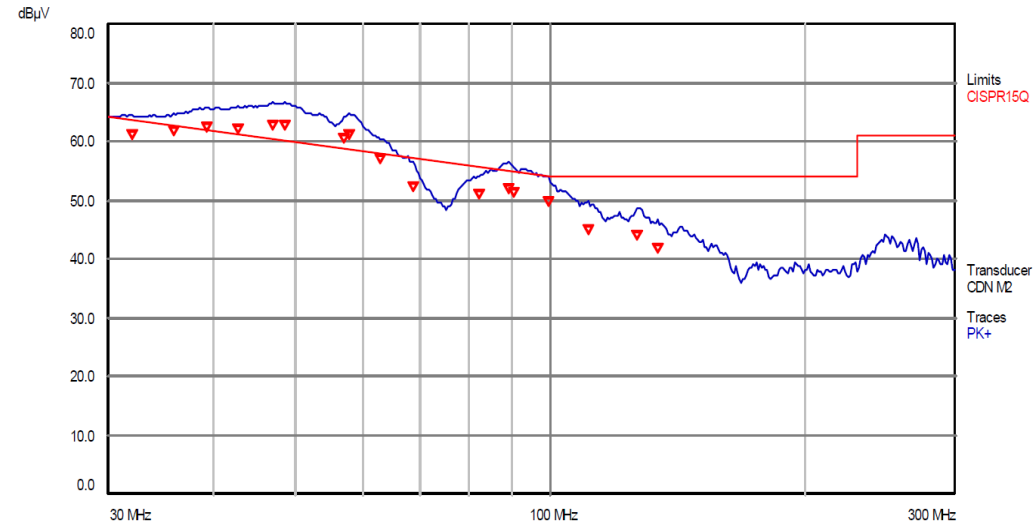
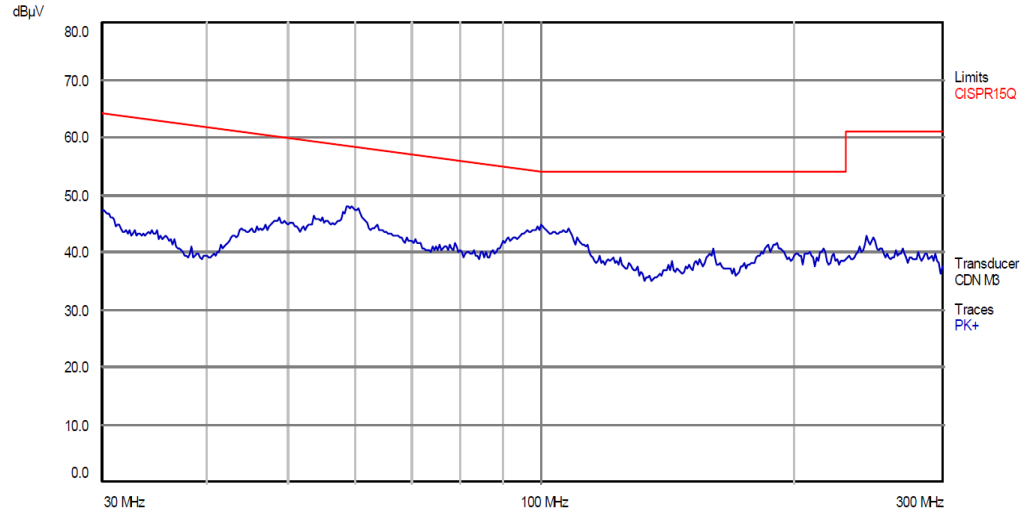


Figure B. 6. *Radiated emission pre-measurement results of DIA4, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

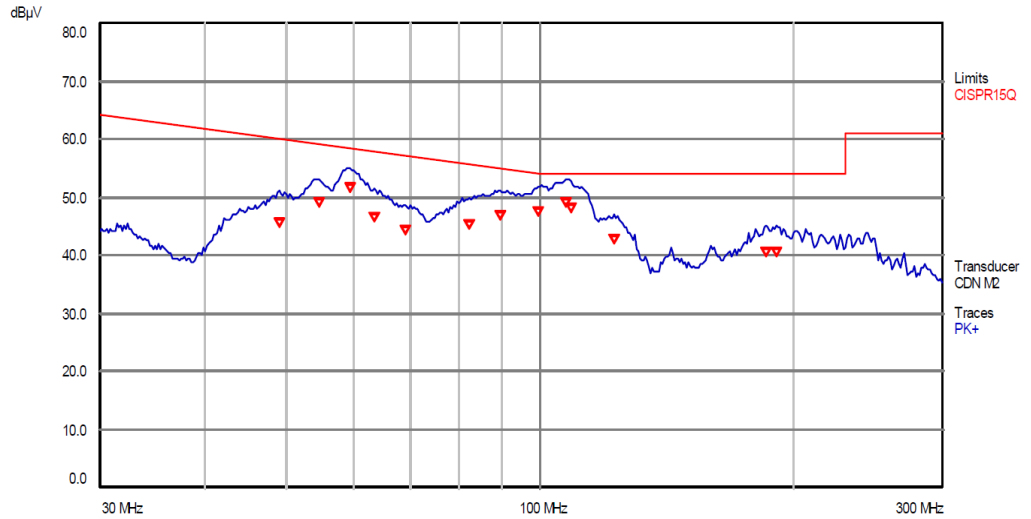
Table B.6. *Radiated emission final measurement results of DIA4.*

With ground					
1	QP	43.24	48.13	60.96	-12.83
1	QP	47.52	49.70	60.18	-10.48
1	QP	48.48	49.43	60.01	-10.58
1	QP	52.44	46.47	59.36	-12.89
1	QP	58.12	46.64	58.51	-11.87
Metal plate					
1	QP	31.32	52.62	63.64	-11.02
1	QP	35.92	52.33	62.50	-10.17
1	QP	39.24	52.71	61.77	-9.06
1	QP	42.52	52.70	61.10	-8.40
1	QP	47.36	53.74	60.21	-6.47
1	QP	48.16	53.68	60.07	-6.39
1	QP	53.8	52.02	59.15	-7.13
1	QP	58.24	53.27	58.49	-5.22
1	QP	62.68	48.40	57.88	-9.48
1	QP	82.52	43.98	55.60	-11.62
1	QP	83.24	44.02	55.52	-11.50
1	QP	99.32	43.37	54.06	-10.69
1	QP	99.56	43.31	54.04	-10.73
1	QP	113.36	44.20	54.00	-9.80
1	QP	119.48	41.91	54.00	-12.09
1	QP	193.96	39.07	54.00	-14.93
Wooden board					
1	QP	32.04	60.29	63.45	-3.16
1	QP	35.92	60.89	62.50	-1.61
1	QP	39.24	61.59	61.77	-0.18
1	QP	42.8	61.39*	61.05	0.34
1	QP	46.96	62.05*	60.28	1.770
1	QP	48.64	61.83*	59.99	1.840
1	QP	57.08	59.65*	58.66	0.99
1	QP	57.88	60.20*	58.54	1.660
1	QP	63.04	56.07	57.83	-1.76
1	QP	68.84	51.43	57.10	-5.67
1	QP	82.48	50.04	55.60	-5.56
1	QP	89.2	51.01	54.95	-3.94
1	QP	90.64	50.58	54.82	-4.24
1	QP	99.4	48.83	54.05	-5.22
1	QP	111.08	44.14	54.00	-9.86
1	QP	126.72	43.30	54.00	-10.70
1	QP	134.04	41.04	54.00	-12.96

a)



b)



c)

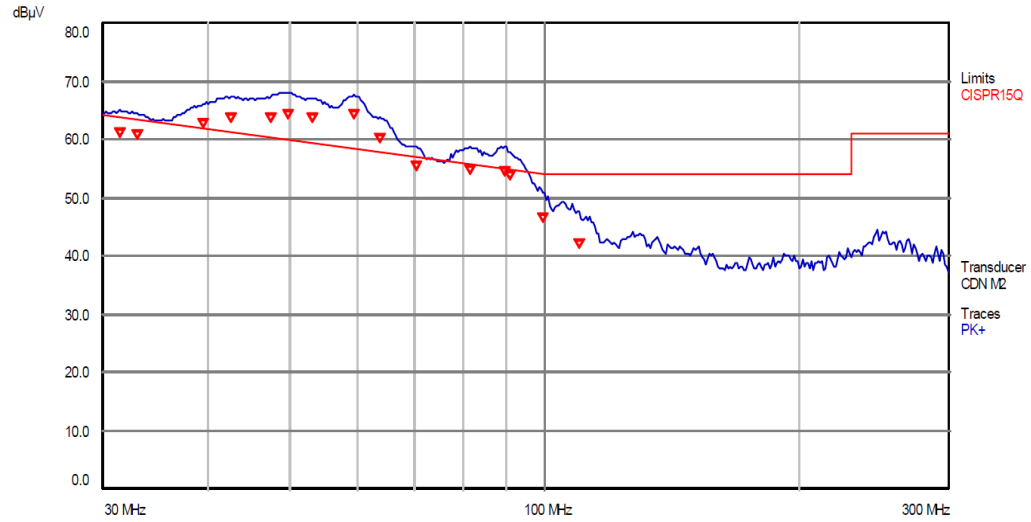
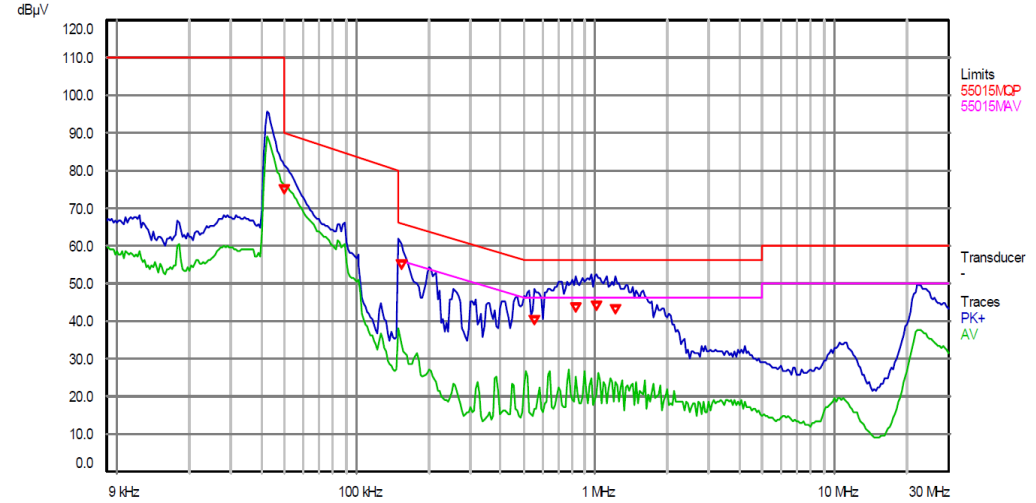


Figure B. 7. *Radiated emission pre-measurement results of DIB5, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

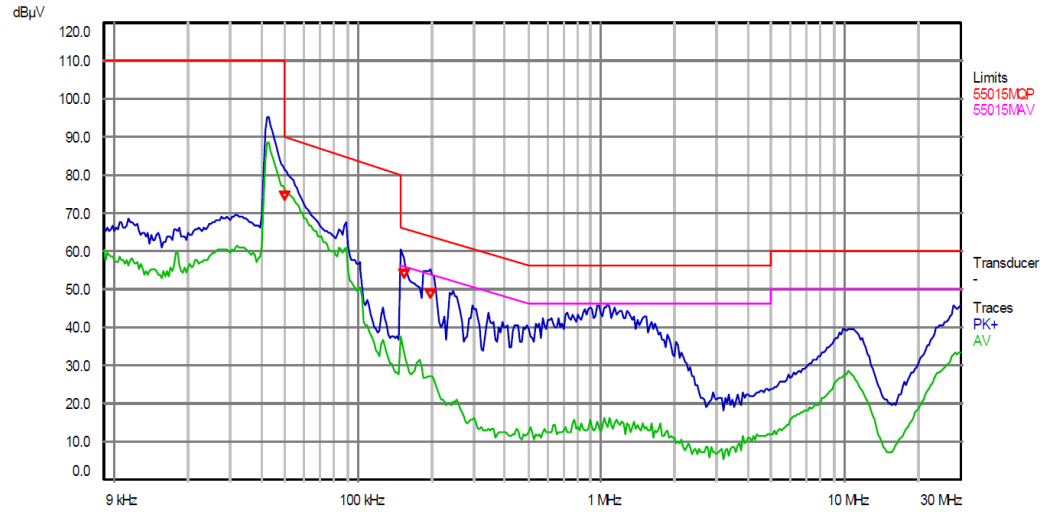
Table B.7. *Radiated emission final measurement results of DIB5.*

Metal plate					
1	QP	49.12	44.89	59.90	-15.01
1	QP	54.6	48.20	59.03	-10.83
1	QP	59.6	50.68	58.30	-7.62
1	QP	63.64	45.75	57.75	-12.00
1	QP	69.04	43.43	57.08	-13.65
1	QP	82.16	44.49	55.63	-11.14
1	QP	89.72	46.19	54.90	-8.71
1	QP	99.32	46.73	54.06	-7.33
1	QP	107.04	48.20	54.00	-5.80
1	QP	109.0	47.19	54.00	-6.81
1	QP	122.6	41.81	54.00	-12.19
1	QP	185.64	39.70	54.00	-14.30
1	QP	190.6	39.54	54.00	-14.46
Wooden board					
1	QP	31.48	60.23	63.60	-3.37
1	QP	33.0	59.97	63.21	-3.24
1	QP	39.48	61.96*	61.72	0.24
1	QP	42.52	62.78*	61.10	1.680
1	QP	47.36	62.81*	60.21	2.600
1	QP	49.64	63.55*	59.82	3.730
1	QP	53.12	62.90*	59.25	3.650
1	QP	59.52	63.56*	58.31	5.250
1	QP	63.96	59.24*	57.71	1.530
1	QP	70.44	54.51	56.91	-2.40
1	QP	81.68	54.06	55.68	-1.62
1	QP	89.64	53.71	54.91	-1.20
1	QP	90.8	53.14	54.80	-1.66
1	QP	99.52	45.56	54.04	-8.48
1	QP	109.68	41.14	54.00	-12.86

a)



b)



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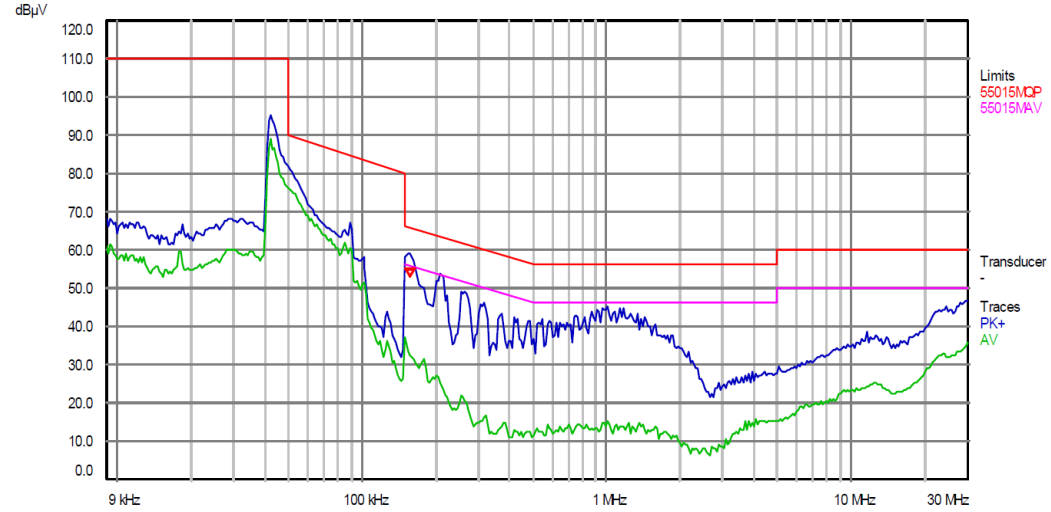


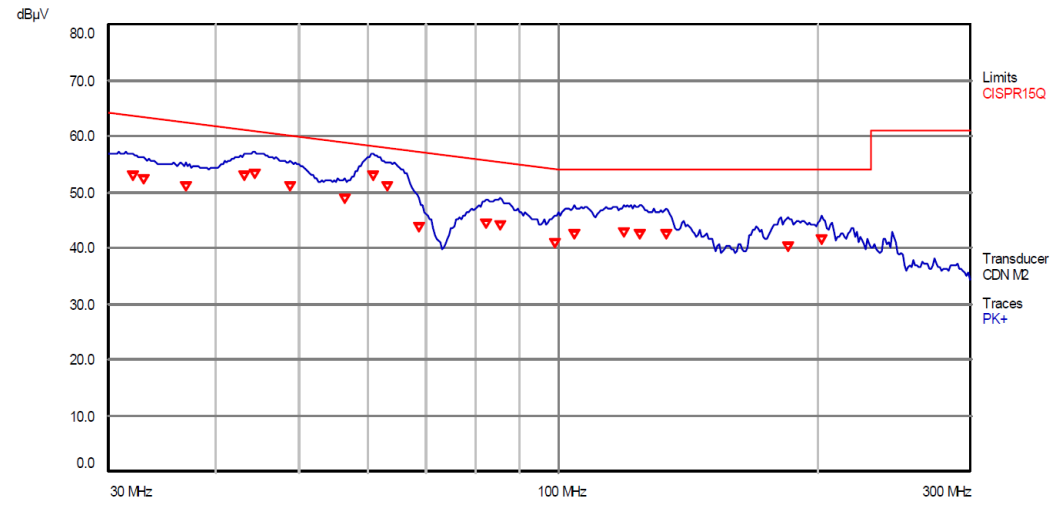
Figure B. 8. *Conducted emission pre-measurement results of DIB5, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

Table B.8. *Conducted emission final measurement results of DIB5.*

With ground					
1	QP	0.05004	73.77	89.99	-16.22
1	QP	0.154	53.75	65.78	-12.03
1	QP	0.554	39.27	56.00	-16.73
1	QP	0.826	42.62	56.00	-13.38
1	QP	1.014	42.75	56.00	-13.25
1	QP	1.214	41.85	56.00	-14.15
Metal plate					
1	QP	0.05004	73.46	89.99	-16.53
1	QP	0.154	52.64	65.78	-13.14
1	QP	0.198	47.43	63.69	-16.26
Wooden board					
1	QP	0.158	52.89	65.57	-12.68

a)

b)



c)

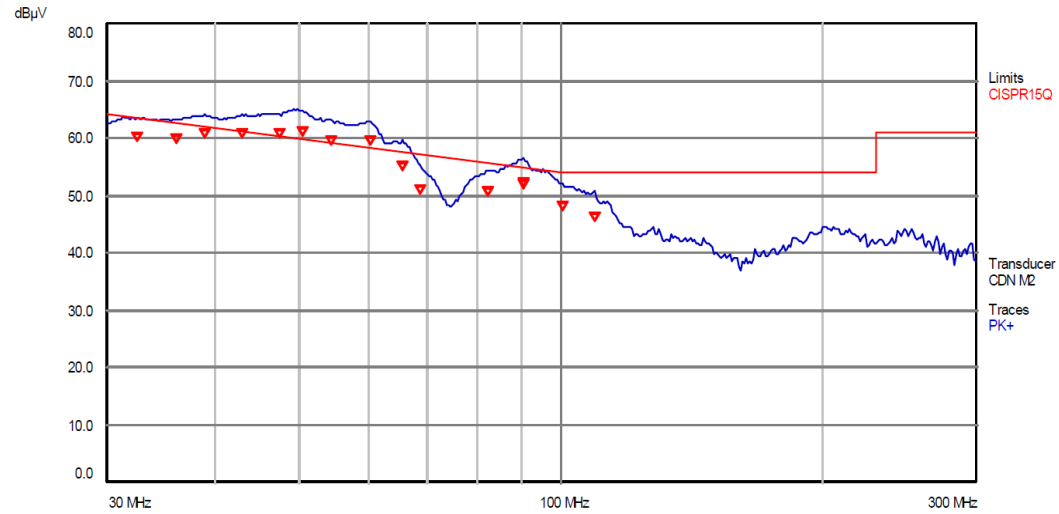
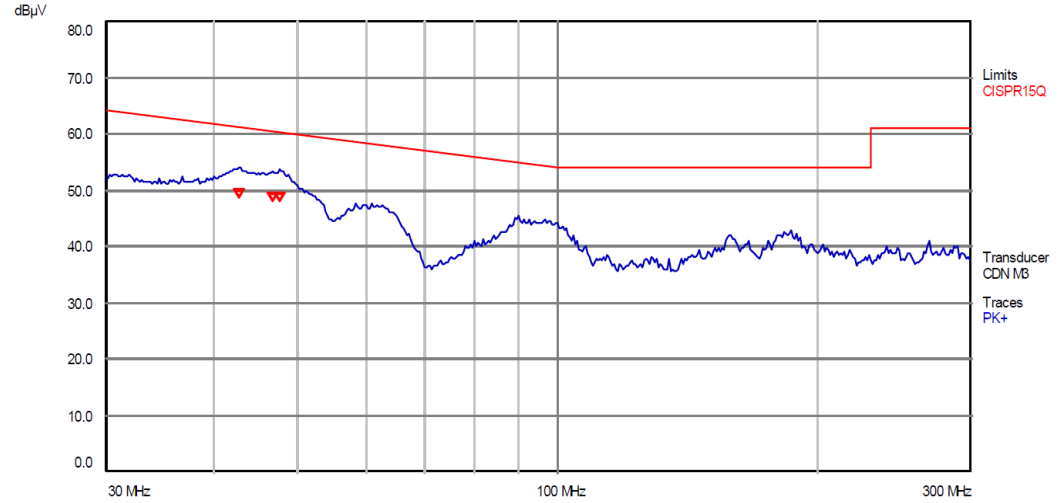


Figure B. 9. *Radiated emission pre-measurement results DIB6, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

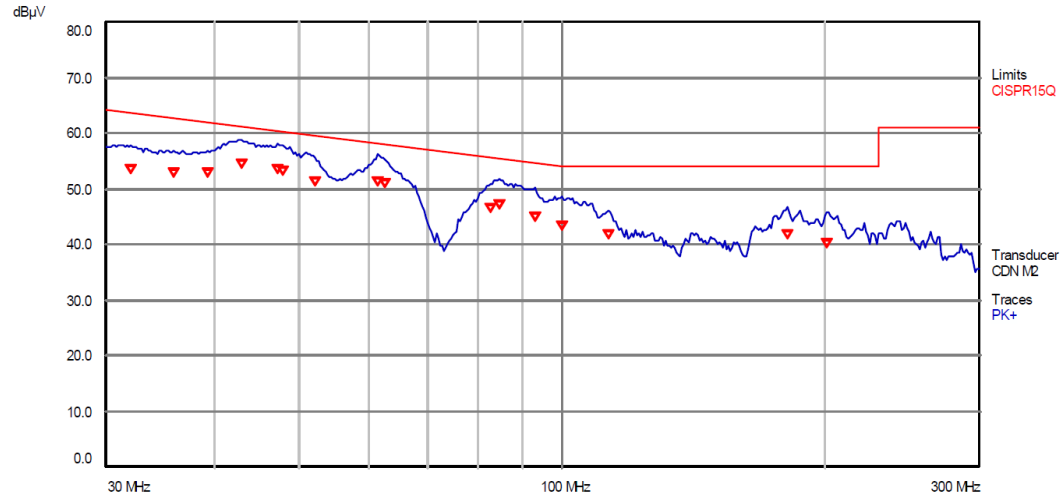
Table B.9. *Radiated emission final measurement results of DIB6.*

With ground											
1	QP	43.24	47.38	60.96	-13.58						
1	QP	46.36	47.37	60.38	-13.01						
1	QP	48.32	45.80	60.04	-14.24						
1	QP	61.28	45.14	58.07	-12.93						
1	QP	62.72	44.35	57.87	-13.52						
Metal plate						Wooden board					
1	QP	32.08	51.97	63.44	-11.47	1	QP	32.48	59.33	63.34	-4.01
1	QP	32.92	51.51	63.23	-11.72	1	QP	36.04	59.07	62.48	-3.41
1	QP	36.96	50.24	62.27	-12.03	1	QP	38.96	60.02	61.83	-1.81
1	QP	43.2	52.17	60.97	-8.80	1	QP	42.92	59.86	61.03	-1.17
1	QP	44.4	52.35	60.74	-8.39	1	QP	47.4	60.04	60.20	-0.16
1	QP	48.72	50.27	59.97	-9.70	1	QP	50.48	60.26*	59.68	0.58
1	QP	56.48	47.82	58.74	-10.92	1	QP	54.44	58.70	59.05	-0.35
1	QP	60.88	52.04	58.12	-6.08	1	QP	60.4	58.81*	58.19	0.62
1	QP	63.2	50.18	57.81	-7.63	1	QP	65.72	54.44	57.49	-3.05
1	QP	68.76	42.97	57.11	-14.14	1	QP	68.92	50.21	57.09	-6.88
1	QP	82.52	43.57	55.60	-12.03	1	QP	82.48	49.89	55.60	-5.71
1	QP	85.68	43.21	55.28	-12.07	1	QP	90.52	51.31	54.83	-3.52
1	QP	99.08	39.96	54.08	-14.12	1	QP	90.6	51.25	54.82	-3.57
1	QP	104.04	41.67	54.00	-12.33	1	QP	100.44	47.16	54.00	-6.84
1	QP	119.24	42.00	54.00	-12.00	1	QP	109.12	45.25	54.00	-8.75
1	QP	124.24	41.48	54.00	-12.52						
1	QP	133.08	41.64	54.00	-12.36						
1	QP	184.4	39.35	54.00	-14.65						
1	QP	201.48	40.66	54.00	-13.34						

a)



b)



c)

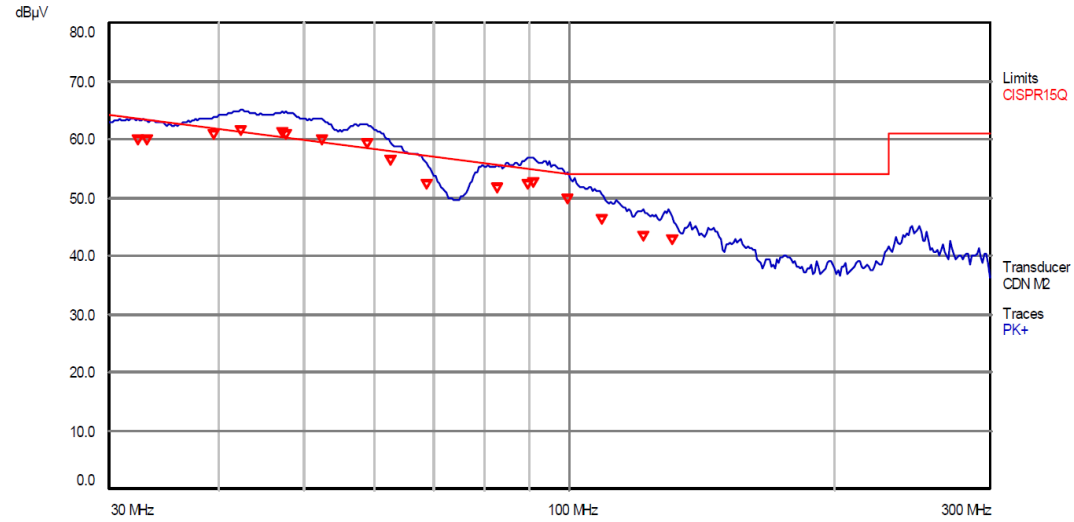
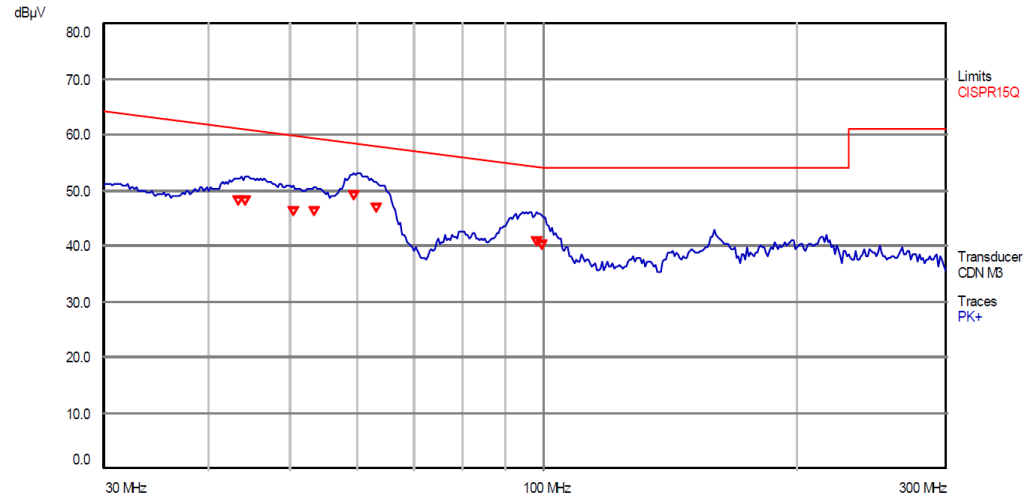


Figure B. 10. *Radiated emission pre-measurement results of DIB7, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

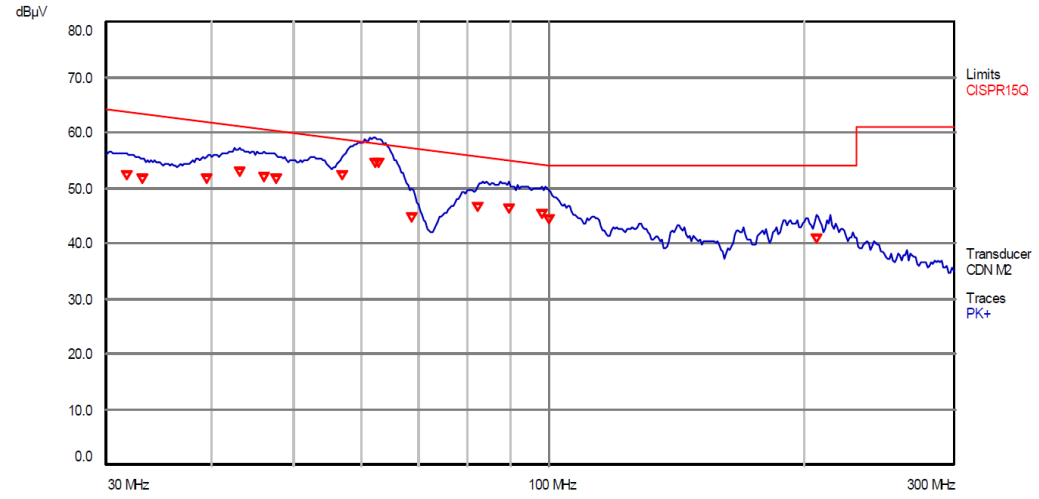
Table B.10. *Radiated emission final measurement results of DIB7.*

With ground					
1	QP	42.76	48.53	61.06	-12.53
1	QP	46.68	47.97	60.33	-12.36
1	QP	47.6	48.05	60.17	-12.12
Metal plate					
1	QP	32.12	52.57	63.43	-10.86
1	QP	35.84	52.08	62.52	-10.44
1	QP	39.32	52.08	61.75	-9.67
1	QP	42.88	53.55	61.03	-7.48
1	QP	47.16	52.61	60.24	-7.63
1	QP	47.8	52.39	60.13	-7.74
1	QP	52.16	50.56	59.41	-8.85
1	QP	61.56	50.56	58.03	-7.47
1	QP	62.72	50.02	57.87	-7.85
1	QP	82.56	45.77	55.59	-9.82
1	QP	84.56	46.46	55.39	-8.93
1	QP	92.92	44.28	54.61	-10.33
1	QP	99.88	42.61	54.01	-11.40
1	QP	112.84	40.96	54.00	-13.04
1	QP	181.08	40.82	54.00	-13.18
1	QP	201.28	39.24	54.00	-14.76
Wooden board					
1	QP	32.4	59.18	63.36	-4.18
1	QP	33.16	59.06	63.17	-4.11
1	QP	39.36	59.94	61.74	-1.80
1	QP	42.36	60.56	61.13	-0.57
1	QP	47.12	60.17	60.25	-0.08
1	QP	47.6	60.11	60.17	-0.06
1	QP	52.44	59.07	59.36	-0.29
1	QP	58.8	58.43*	58.41	0.02
1	QP	62.68	55.49	57.88	-2.39
1	QP	68.8	51.49	57.11	-5.62
1	QP	82.56	50.73	55.59	-4.86
1	QP	89.52	51.57	54.92	-3.35
1	QP	90.72	51.62	54.81	-3.19
1	QP	99.52	49.03	54.04	-5.01
1	QP	109.0	45.55	54.00	-8.45
1	QP	121.36	42.43	54.00	-11.57
1	QP	131.04	41.76	54.00	-12.24

a)



b)



c)

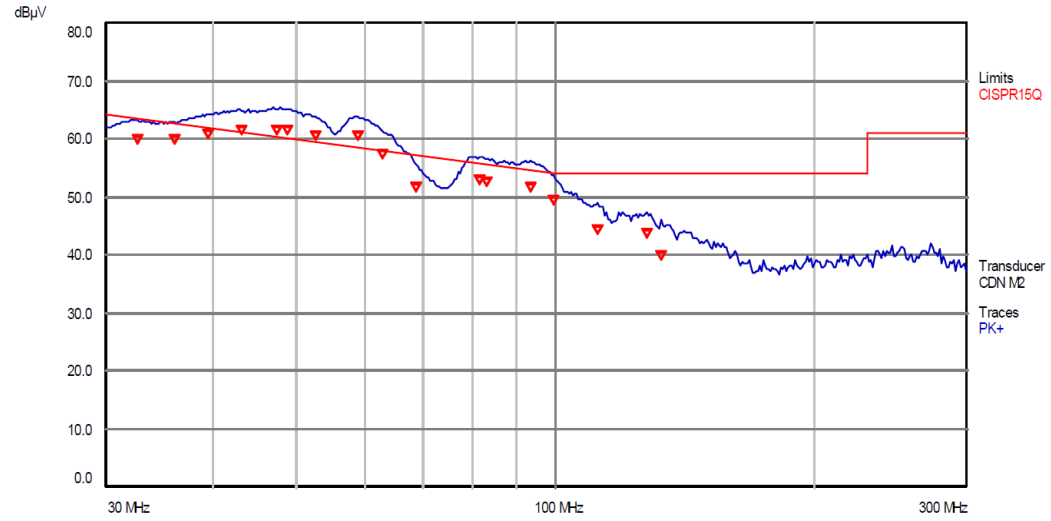


Figure B. 11. *Radiated emission pre-measurement results of DIB8, a) with ground on the metal plate, b) without ground on the metal plate and c) without ground on the wooden board.*

Table B.11. *Radiated emission final measurement results of DIB8.*

With ground											
1	QP	43.32	47.28	60.95	-13.67						
1	QP	44.12	47.38	60.80	-13.42						
1	QP	50.48	45.28	59.68	-14.40						
1	QP	53.4	45.33	59.21	-13.88						
1	QP	59.6	48.39	58.30	-9.91						
1	QP	63.32	46.06	57.80	-11.74						
1	QP	98.16	39.97	54.15	-14.18						
1	QP	99.6	39.49	54.03	-14.54						
Metal plate						Wooden board					
1	QP	31.68	51.54	63.55	-12.01	1	QP	32.68	59.10	63.29	-4.19
1	QP	33.12	50.91	63.18	-12.27	1	QP	36.0	58.93	62.49	-3.56
1	QP	39.4	50.70	61.74	-11.04	1	QP	39.36	60.04	61.74	-1.70
1	QP	43.08	52.11	60.99	-8.88	1	QP	43.16	60.56	60.98	-0.42
1	QP	46.16	51.22	60.42	-9.20	1	QP	47.52	60.79*	60.18	0.61
1	QP	47.72	50.91	60.14	-9.23	1	QP	48.72	60.73*	59.97	0.76
1	QP	57.12	51.51	58.65	-7.14	1	QP	52.52	59.78*	59.35	0.43
1	QP	62.44	53.79	57.91	-4.12	1	QP	59.04	59.71*	58.38	1.330
1	QP	62.92	53.80	57.85	-4.05	1	QP	62.84	56.50	57.86	-1.36
1	QP	68.96	43.81	57.09	-13.28	1	QP	68.84	50.94	57.10	-6.16
1	QP	82.52	45.59	55.60	-10.01	1	QP	81.72	51.96	55.68	-3.72
1	QP	89.76	45.55	54.90	-9.35	1	QP	83.0	51.84	55.55	-3.71
1	QP	98.12	44.46	54.16	-9.70	1	QP	93.36	50.86	54.57	-3.71
1	QP	100.04	43.59	54.00	-10.41	1	QP	99.4	48.47	54.05	-5.58
1	QP	206.96	40.12	54.00	-13.88	1	QP	111.72	43.39	54.00	-10.61
						1	QP	128.0	42.71	54.00	-11.29
						1	QP	132.68	39.20	54.00	-14.80